8

180

180

-: HAND WRITTEN NOTES:-

OF

4

ELECTRONICS & COMMUNICATION ENGINEERING

4

-: SUBJECT:-

DIGITAL ELECTRONICS

8

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②

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BOOLEAN ALGEBRA.

⇒ Boolean Algebra :-

(·) when no. of variable are less. (1,2,3)

(·) It is preffered when output is 0 or 1. ③

⇒ K - map :-

(·) when no. of variables are 2,3,4,5 (upto 5 variable)

(·) output is 0, 1 or, x.

⇒ Tabulation method.

(·) It is used when no. of variables are more.

Boolean Algebra :- ③

⇒ A complement → $\bar{A}$ or, A'

$\bar{\bar{A}} = A$

⇒ NOT :-

0 = 1

1 = 0

⇒ AND :-

$0 \cdot 0 = 0$ $\qquad A \cdot A = A$

$0 \cdot 1 = 0$ $\qquad A \cdot 1 = A$

$1 \cdot 0 = 0$ $\qquad A \cdot 0 = 0$

$1 \cdot 1 = 1$ $\qquad A \cdot \bar{A} = 0$

⇒ OR :-

$0+0 = 0$ $\qquad A + A = A$

$0+1 = 1$ $\qquad A + 1 = 1$

$1+0 = 1$ $\qquad A + 0 = A$

$1+1 = 1$ $\qquad A + \bar{A} = 1$

Problem:- $AB + A\bar{B}$

Sol:- $A(B + \bar{B})$ $\qquad (\because B + \bar{B} = 1)$

$= A$

classmate

oblem:- $AB + A\bar{B}C + A\bar{B}\bar{C}$, find the min. no. of NAND Gate.

option. [✓ (a) 0] (b) 1

(c) 2 (d) 3.

y

y

Sol^n :- $AB + A\bar{B}C + A\bar{B}\bar{C}$

$= AB + A\bar{B}(C+\bar{C})$

$= AB + A\bar{B}$ $(\because C+\bar{C} = 1)$

$= A(\bar{B}+B)$

$= A$

NO NAND gate required.

Advantage of Minimization :-

⇒ No. of logic gate ↓

⇒ Speed ↑

⇒ Power dissipation ↓

⇒ complexity of circuit less

⇒ fan in ↓ (no. of input ↓)

⇒ Cost ↓.

Problem:- Simplify :-

(a) $A\bar{B} + AB\bar{C} + A\bar{B}\bar{C}D$

Sol^n :- $A\bar{B}\bar{C} + A\bar{B}(1+\bar{C}D)$

$= AB\bar{C} + A\bar{B}$ $(1 + x = 1)$

$= A(\bar{B} + B\bar{C})$ $(\because \bar{B} + B\bar{C} = \bar{B} + \bar{C})$

$= A(\bar{B}+\bar{C})$

$= A\bar{B} + A\bar{C}$

(b) $(A+B)(A+C)$

Sol^n :- $A \cdot A + A \cdot C + AB + BC$

$= A + A(C+B) + BC$

$= A(1+B+C) + BC$

$= A + BC$

$$\boxed{(A+B)(A+C) = A+BC}$$

Transposition Theorem

classmate

PAGE

Similarly :

$$\boxed{(\bar{x}+y)(\bar{x}+z) = \bar{x}+yz}$$

(c) $(A+B+C)(A+\bar{B}+C)(A+B+\bar{C})$

⑤

Sol: take $A+B = X$

$= (X+C)$ ~~$(A+\bar{B}+C)$~~ $(X+\bar{C})$

$= (X+C\bar{C})(A+\bar{B}+C)$

$= X(A+\bar{B}+C)$

$= (A+B)(A+\bar{B}+C)$

$= A+B(\bar{B}+C)$

$= A+B\bar{B}+BC$

$= A+BC$

(d) $(A+B)(A+\bar{B})(\bar{A}+B)(\bar{A}+\bar{B})$

Sol: $(A+B)(A+\bar{B})\quad(\bar{A}+B)(\bar{A}+\bar{B})$

$= (A+B\bar{B})\cdot(\bar{A}+B\bar{B})$

$= (A)(\bar{A})$

$= 0$

$\boxed{A+BC = (A+B)(A+C)}$ Distribution theorem.

(e) $A+\bar{A}B$

Sol $(A+\bar{A})(A+B)$

$= 1(A+B) = A+B$.

(f) $A+\bar{A}\bar{B}$

Sol: $(A+\bar{A})(A+\bar{B})$

$= 1(A+\bar{B}) = A+\bar{B}$

(g) $AB+\bar{A}\bar{B}+A\bar{B}$

Sol: $A(B+\bar{B})+\bar{A}\bar{B}$

$= A+\bar{A}\bar{B}$

$= (A+\bar{A})(A+\bar{B})$

$= A+\bar{B}$ Ans

(h) $AB + \bar{A}B + A\bar{B}$

Sol^n :- $B(A+\bar{A}) + A\bar{B}$

$= B + A\bar{B}$

$= (B+A)(B+\bar{B})$

$= A+B$ Ans.

(i) $AB\bar{C} + ABC + \bar{A}BC$

Sol^n :- $AB\bar{C} + ABC + ABC + \bar{A}BC$ $(\because A+A = A)$

$= AB(C+\bar{C}) + (A+\bar{A})BC$

$= AB + BC$

$= B(A+C)$

(j) $AB + \bar{A}C + BC \longrightarrow$ redundant term.

Sol^n :- $AB + \bar{A}C + BC(A+\bar{A})$

$= AB + \bar{A}C + BCA + \bar{A}BC$

$= AB(1+C) + \bar{A}C(1+B)$

$= AB + \bar{A}C$

Note :- In this case BC is known as redundant term i.e. not used or not compulsory term.

⇒ $AB + \bar{A}C + BC = AB + \bar{A}C$, called consensus theorem or redundancy theorem.

⇒ Shortcut method :-

(a) Three variable.

(b) each variable comes twice.

(c) one variable is complemented.

(K) $AB + B\underline{\bar{C}} + A\underline{C}$

Sol^n :- $B\bar{C} + AC$ { The term which is complemented is taken.

(L) $A\bar{B} + BC + AC$

Sol^n :- $A\bar{B} + BC$

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(m) $(\underline{A}+B)(\bar{\underline{A}}+C)(B+C)$

Sol: $(A+B)(\bar{A}+C)$, $\because (B+C)$ is redundant term.

(n) $(A+\underline{B})(\bar{\underline{B}}+C)(A+C)$

Sol: $(A+B)(\bar{B}+C)$

1 ⑦

(o) $\bar{\underline{A}}\bar{B} + \underline{A}\bar{C} + \bar{B}\bar{C}$

Sol: In this case all the variable are complemented only one are uncomplemented then.

$= \bar{A}\bar{B} + A\bar{C}$ ($\because$ The term which is uncomplemented is taken)

(p) $\bar{A}\bar{B} + \bar{B}C + \bar{A}\bar{C}$

Sol: $\bar{B}C +$ ~~$\bar{A}\bar{B}$~~ $\bar{A}\bar{C}$

(q) $(\bar{A}+\bar{B})(\bar{B}+\bar{\underline{C}})(\bar{A}+\underline{C})$

Sol: $(\bar{B}+\bar{C})(\bar{A}+C)$

$\overline{ABC}$	$=$	$\bar{A}+\bar{B}+\bar{C}$
$\overline{A+B+C}$	$=$	$\bar{A}\cdot\bar{B}\cdot\bar{C}$

Demorgan's theorem.

Boolean Algebra :-

↳ Minimization

⇒ SOP → minimal
→ canonical

⇒ POS → minimal
→ canonical

⇒ Dual

⇒ Complement Expression

⇒ Truth table

⇒ Venn Diagram

⇒ Switching circuit

⇒ Statement.

(A) Minimization :-

(a) $XY + \overline{XY}WZ$

Sol :- $A = XY$ and $B = WZ$

Then.

$= A + \bar{A}B$

$= (A+\bar{A})(A+B)$

$= A+B$

$= XY + WZ$

(b) let $f(A,B) = \bar{A} + B$ Then the value of

$f\,[f\,(x+y,\ y)\ ,\ z)$ is

(a) $XY + Z$

(b) $X\bar{Y} + Z$ ✓

(c) $\bar{X}Y + Z$

(d) X

Sol :- $f\,[f\{(x+y), y\},\ z]$

$= F\,[\ \overline{X+Y} + Y\ ,\ Z\ ]$

$= F\,[\ \bar{X}\cdot\bar{Y} + Y\ ,\ Z\ ]$

$= \overline{\bar{X}\bar{Y} + Y} + Z$

$= \overline{\bar{X}\bar{Y}} \cdot \bar{Y} + Z$

$= (\bar{\bar{X}} + \bar{\bar{Y}})\bar{Y} + Z$

$= X\bar{Y} + Y\bar{Y} + Z$

$= X\bar{Y} + Z$ Ans.

(c) let $X * Y = \bar{X} + Y$ and $Z = X * Y$

Then the value of $Z * X$ is

(a) X

(b) 1

(c) 0

(d) $\bar{X}$

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(B) SOP (Sum of Product Form)

$\underbrace{ABC} + \underbrace{\bar{A}BC} + \underbrace{AB\bar{C}}_{\hookrightarrow \text{ minterm}}$

⇒ In SOP Form, each product term is known as Minterm or Implicant.

⇒ Sop Form is used when O/P of logical expression is 1.
(means $1 \rightarrow A$ and $0 \rightarrow \bar{A}$)

Ex :- $5 \rightarrow 101 \rightarrow A\bar{B}C$

$9 \rightarrow 1001 \rightarrow A\bar{B}\bar{C}D$

Ques :- For the given truth table, minimize SOP expression.

	A	B	Y
$\bar{A}\bar{B}$	0	0	1 ✓
	0	1	0
$A\bar{B}$	1	0	1 ✓
	1	1	0

Sol :- In SOP form only 1 taken.

$= \bar{A}\bar{B} + A\bar{B}$

$= \bar{B}\,(\bar{A} + A)$

$= \bar{B}$

⇒ Y can written as :-

$Y(A, B) = \Sigma m(0, 2)$

Ques :- Simplified the expression for

$Y(A, B) = \Sigma m(0, 2, 3)$
00 10 11

Sol :- logical expression in sop form :-

$Y = \bar{A}\bar{B} + A\bar{B} + AB$

$= \bar{B}\,(\bar{A} + A) + AB$

$= \bar{B} + AB$

$= (\bar{B} + A)\,(\bar{B} + B)$

$= A + \bar{B}$

$= A + \bar{B}$

SOP can be of two form.

(1) Minimal form

(2) canonical form.

⇒ $A + \bar{A}B = A + B$ (It is a minimal form)

⇒ In canonical form, each term must have all variable.

e.g. $A + \bar{A}B$

$= A(B+\bar{B}) + \bar{A}B$

$= AB + A\bar{B} + \bar{A}B$.

Thus each min-term will contain all variable.

IS-2003

Problem:- In canonical SOP form, no. of min term presenting the logical expression $A + \bar{B}C$ is.

(a) 4 (c) 6

✓ (b) 5 (d) 7

Sol^n:-

$A + \bar{B}C$

$= A(B+\bar{B})(C+\bar{C}) + \bar{B}C(A+\bar{A})$

$= (AB + A\bar{B})(C+\bar{C}) + A\bar{B}C + \bar{A}\bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + A\bar{B}C + \bar{A}\bar{B}C$

$= ABC + AB\bar{C} + A\bar{B}C + A\bar{B}\bar{C} + \bar{A}\bar{B}C$

i.e. 5 terms.

(C) POS Form (Product of Sum) :-

$(A+B+\bar{C})\ (\bar{A}+B+C)\ (A+B+C)$

↳ max term

⇒ POS form are used when O/P is logic '0'.

$0 \rightarrow A$

$1 \rightarrow \bar{A}$

Ex :- $5 \rightarrow 101 \rightarrow \bar{A}B\bar{C}$

$9 \rightarrow 1001 \rightarrow \bar{A}BC\bar{D}$

Ques:- For a given th truth table minimize POS expression.

	A	B	Y
	0	0	1
$A+\bar{B}$	0	1	0 ✓
	1	0	1
$\bar{A}+\bar{B}$	1	1	0 ✓

Sol:- we take only that value at which O/P is '0'.

$Y = (A+\bar{B})\ (\bar{A}+\bar{B})$

$= \bar{B} + A\bar{A}$

$= \bar{B}$

⇒ Y can be written in POS form as,

$Y(A,B) = \Pi M(1,3) = \bar{B}$

and for SOP :-

$Y(A,B) = \Sigma m(0,2) = \bar{B}$

i.e.

$\Sigma m(0,2) = \Pi M(1,3)$

⇒ If $F(A,B,C) = \Sigma m(0,1,4,7)$

There are 3 variable then 8 combination then max term are, 2,3,5,6.

$F(A,B,C) = \Sigma m(0,1,4,7) = \Pi M(2,3,5,6)$

⇒ with 'n' variable, maximum possible minterms or maxterms are 2^n. eg.

(i) for, $n = 2$. i.e. (A, B)

Total no. of min or max terms are $2^2 = 4$.

(ii) for, $n = 3$ i.e. (A, B, C)

Total no. of min or max terms are $2^3 = 8$.

⇒ For $n = 2$, (A, B) total 16 logical expression i.e.

1	A	$A\bar{B}$	AB
0	$\bar{A}$	$\bar{A}B$	$A+B$
$\bar{A}B + A\bar{B}$	B	$A+\bar{B}$	$\bar{A}\bar{B}$
$AB + \bar{A}\bar{B}$	$\bar{B}$	$\bar{A}+B$	$\bar{A}+\bar{B}$

Note :- With n variable maximum possible logical expression are 2^{2^n}.

eg. for $n = 2$, logical expression $= 2^{2^2} = 16$

for $n = 3$ $= 2^{2^3} = 256$

IES-2004
GATE-2002
ISRO-2001
ISRO-2002

Problem :- For $n = 4$ what is the total no. of logical expression.

Sol^n :- logical expression $= 2^{2^4}$

$= 2^{16} = 35536.$

(D) Dual Form :-

+ive logic

⇒ +ive logic means higher voltage corresponds to logic '1'.

⇒ logic '0' → 0 v

logic '1' → +5v

−ive logic

⇒ −ive logic means higher voltage corresponds to logic '0'.

⇒ logic 0 = +5V

logic 1 = 0V

Ques:- logic 0 → −5v

logic 1 → 0v

Sol:- Higher value of voltage (0V) for logic 1. then +ive logic.

Ques:- ECL :

logic '0' → −1.7V

logic 1 → −0.8V

Sol:- −0.8V is larger value than −1.7V then it is +ive logic.

+ive logic AND

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

−ive logic AND

A	B	Y
1	1	1
1	0	1
0	1	1
0	0	0

+ive logic OR

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

−ive logic OR

A	B	Y
1	1	1
1	0	0
0	1	0
0	0	0

⇒ For −ive logic or gate, convert 1 to 0 and 0 to 1.

⇒ we can say that +ive logic AND gate is equal to −ive logic OR gate and −ive logic AND gate is equal to +ive logic OR gate.

⇒ Dual expression is used to convert +ive logic into -ive logic or, -ive logic to +ive logic.

⇒ $AB \xrightarrow{\text{Dual}} A+B$

Dual is nothing but -ive logic.

⇒ $\text{AND} \xrightarrow[\text{Dual}]{\text{-ive logic}} \text{OR}$

⇒ $\text{OR} \xrightarrow[\text{Dual}]{\text{-ive logic}} \text{AND}$

(-) AND ⟷ OR
(-) $\cdot \longleftrightarrow +$
(-) $1 \longleftrightarrow 0$
(-) keep variable as it is

} Dual.

em:- Find Dual.

$AB\bar{C} + \bar{A}BC + ABC$

:- Dual :-

$(A+B+\bar{C})(\bar{A}+B+C)(A+B+C)$

if we find again dual then,

$AB\bar{C} + \bar{A}BC + ABC$

⇒ For any logical expression, if two times dual is used resulting same expression.

Self Dual :-

$AB + BC + AC$

Dual :-

$= (A+B)(B+C)(A+C)$

$= (B+AC)(A+C)$

$= BA + BC + AC + AC$

$= AB + BC + AC$ (again same expression)

⇒ In some of the logical expression not all its dual gives the same expression.

⇒ In self Dual expression, if one time dual is used resut in same expression.

$$\boxed{n \text{ variable} \rightarrow \text{self Dual} = 2^{2^{n-1}}}$$

Ie If there are n variables then total no. of self dual expression is $2^{2^{n-1}}$.

eg :-

(i) For $n = 1$. ⇒ $2^{2^{0}} = 2$.

Then 2 dual expression.

A → Self dual → A
Ā → Ā

} Total self dual expression are 2.

(ii) For $n = 2$ ⇒ $2^{2^{1}} = 4$.

Then 4 dual expression.

A → A , B → B
Ā → Ā , B̄ → B̄

(iii) For $n = 3$ ⇒ $2^{2^{3-1}} = 16$.

Then 16 dual expression.

$A, \bar{A}, B, \bar{B}, C, \bar{C}, \bar{A}\bar{B}+\bar{B}\bar{C}+\bar{C}\bar{A}, AB+BC+CA, ---$

(E) Complement :-

if $Y = ABC + \bar{A}BC + A\bar{B}C$

complement is,

$$\bar{Y} = (\bar{A}+\bar{B}+\bar{C})(A+\bar{B}+\bar{C})(\bar{A}+B+\bar{C})$$

(•) AND ⟷ OR
(•) · ⟷ +
(•) 1 ⟷ 0
(•) complement of each variable.

} complement.

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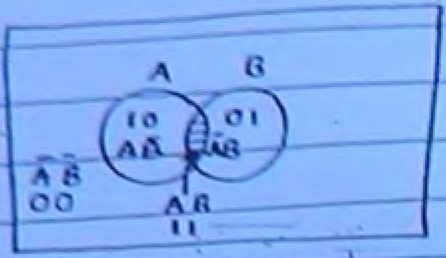
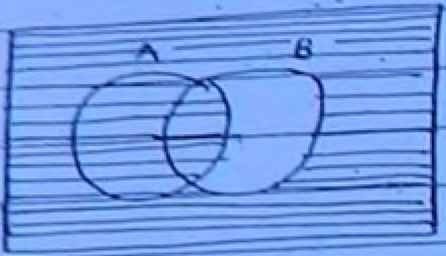
(F) Venn Diagram :-

For two variable (A, B).



Ques :- For a given venn diagram, minimize the SOP expression for shaded region.

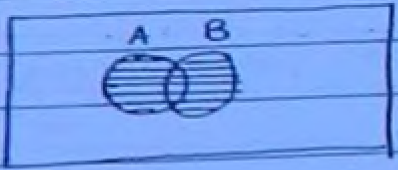


Sol :-

$$Y = \bar{A}\bar{B} + A\bar{B} + AB$$
$$= \bar{B}(\bar{A} + A) + AB$$
$$= \bar{B} + AB$$
$$= (\bar{B} + A)(\bar{B} + B)$$
$$= \underset{\downarrow}{A} + \underset{\downarrow}{\bar{B}}$$

(0 1) for POS form.

Ques :- SOP expression for shaded region.

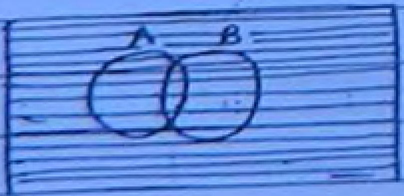


Sol :-

$$Y = AB + A\bar{B} + \bar{A}B$$
$$= A(B + \bar{B}) + \bar{A}B$$
$$= A + \bar{A}B$$
$$= (A + \bar{A})(A + B)$$
$$= \underset{\downarrow}{A} + \underset{\downarrow}{B}$$

$(0, 0) \longrightarrow$ (in POS form)

Ques :- SOP expression



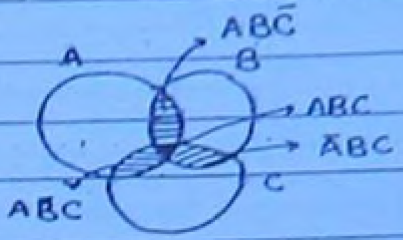
Sol:- $\bar{A}B + A\bar{B} + AB + \bar{A}\bar{B}$

$= B(A+\bar{A}) + \bar{B}(A+\bar{A})$

$= B + \bar{B}$

$= 1.$

⇒ For 3- variable :-



SOP form for shaded portion

$= ABC + \bar{A}BC + AB\bar{C} + A\bar{B}C + \underbrace{ABC + ABC}_{\text{extradded}}$

$= BC(A+\bar{A}) + AB(\bar{C}+C) + AC(B+\bar{B})$

$= AB + BC + CA$

(G) Switching Circuit :-

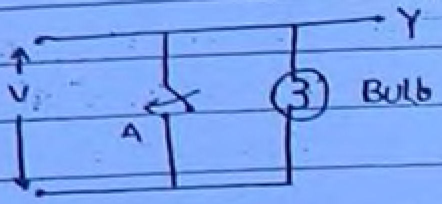
For Series :-

Truth table :-

A	Y
0	0
1	1

For Parallel :-

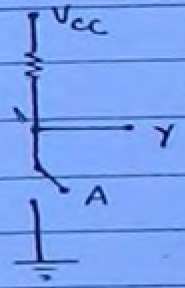
A	Y
0	1
1	0



⇒ In place of bulb if there is resistor then answer remains the same but some drop.

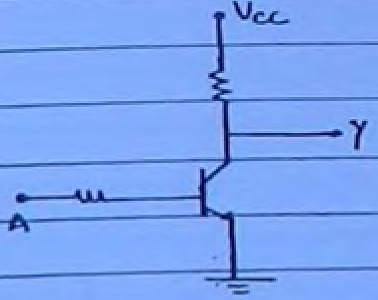
Truth table :-

A	Y
0	1
1	0



⇒ In place of switch if there is a transistor.

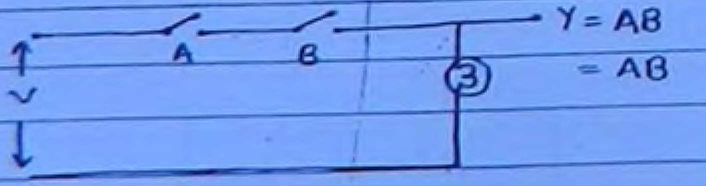
A	Y
0	1
1	0



(i) For A = 1 transistor becomes short circuit.

For two switch A and B :-

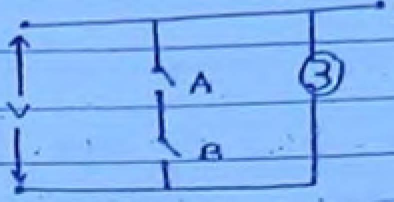
AND ⇒



Y = AB
= AB

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

NAND ⇒

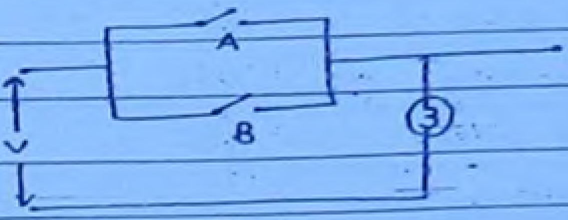


$Y = \overline{AB}$

$= \overline{AB}$

A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

OR ⇒

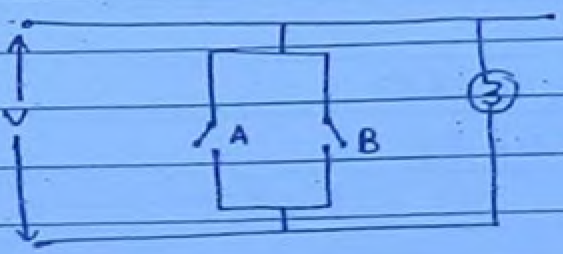


$Y = A+B$

$= A+B$

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

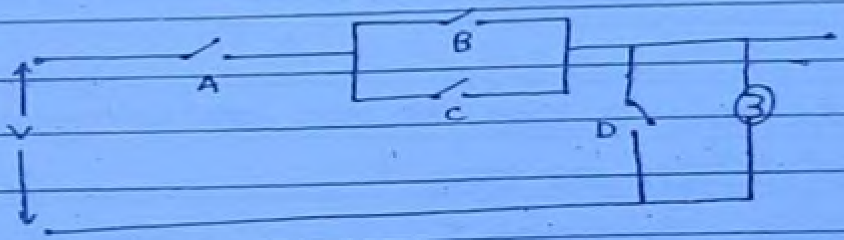
NOR ⇒



$Y = \overline{A+B}$

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Ques:-



Sol:-

$Y = A \cdot (B+C) \cdot \bar{D}$

$= (AB + AC)\,\bar{D}$

$= AB\bar{D} + AC\bar{D}$.

(H). STATEMENT :-

Ques:- A logic circuit have 3 input A, B, C and o/p is Y. o/p Y is 1. for the following combination.

(i) B and C are true = BC

(ii) A and C are false = $\bar{A}\bar{C}$

(iii) A, B and C are true = ABC

(iv) A, B and C are false = $\bar{A}\bar{B}\bar{C}$

then minimize the o/p for Y.

Sol:- o/p Y = 1. (take min term = SOP form)

$$Y = BC + \bar{A}\bar{C} + ABC + \bar{A}\bar{B}\bar{C}$$

$$= BC(1 + A) + \bar{A}\bar{C}(1 + \bar{B})$$

$$= BC + \bar{A}\bar{C}$$

if o/p Y = 0, then take max term (POS form).

Ques:- A logic ckt have 3 input A, B, C and o/p is F = 1. when majority no. of I/ps are logic 1.

- (i) minimizing expression F
- (ii) Implement logic ckt.

Sol:-

A	B	C	F
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1 ✓
1	0	0	0
1	0	1	1 ✓
1	1	0	1 ✓
1	1	1	1 ✓

$$F = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= \bar{A}BC + ABC + ABC + A\bar{B}C + AB\bar{C} + ABC$$

$$= BC(A + \bar{A}) + AC(B + \bar{B}) + AB(\bar{C} + C)$$

$$= AB + BC + CA.$$

(I) LOGIC GATES :-

⇒ Basic Building Blocks

NOT
AND } → Basic gate
OR

NAND } → universal gate
NOR

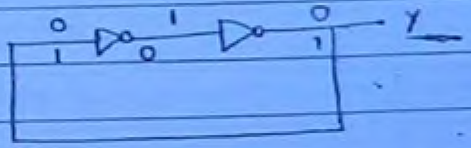
EXOR } → Arithmetic ckt.
EXNOR } comparator, parity generator/checker, code converte
(Binary to gray, Gray to Binary)

NOT :-

A	Y
0	1
1	0

IES-2010
GATE-2010

Ques:- Circuit shown in the fig are



(a) Buffer
(b) Astable MV
[✓ (c)] Bistable MV
(d) square wave generator.

Sol:- If there is no feedback then it is buffer. In Buffer if we apply 0 then get 0
" 1 → " 1.
" no I/P " " no I/P.
Buffer means whatever the I/P ie. the O/P.

⇒ But there is a feedback and the O/P is stable if we give 1 as I/P, O/P is also 1 and if gives 0 then O/P is 0 the two stable state.

⇒ Hence it is Bistable multivibrator.

PAGE
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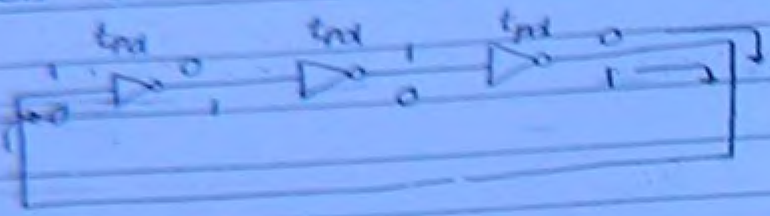
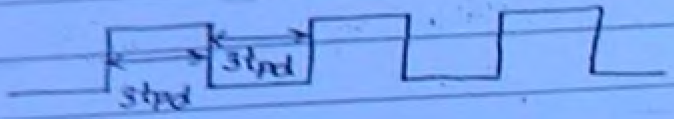
Ques: Ckt shown is



Sol:- t_{pd} = Propagation delay.

"0" for = $3t_{pd}$

1 for = $3t_{pd}$



It is called

(i) Square wave generator.

(ii) As o/p is not stable sometime 1 and sometime 0 Hence it is also called astable multivibrator.

(iii) clock generator

(iv) Ring oscillator.

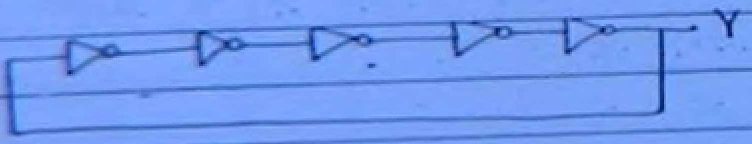
Total time period (T) = $6T_{pd}$

then.

$$\boxed{T = 2N t_{pd}}$$

N = no. of inverters in feedback.

Ques:- In a ckt shown in fig. the propagation delay of each NOT gate is 100 PSec. Then frequency of generator square wave is



(a) 10GHz

(b) 1GHz

(c) 100 MHz

(d) 10 MHz

Sol:- $T = 2Nt_{pd}$

$= 2 \times 5 \times 100$ PSec $=$ 1000 PSec

$f = \frac{1}{T} = \frac{1}{1000 \times 10^{-12}\,sec} = 10^9$ Hz

$=$ 1GHz

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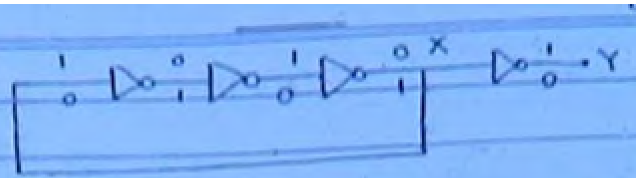
Ques:-



Solⁿ:- The ckt shown in the fig the propogation delay of each NOT gate is 2nsec. Then time period of generated square wave is.

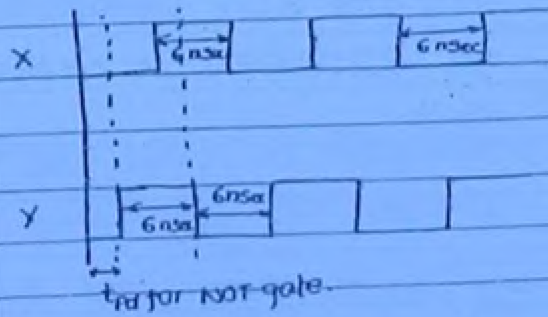
(a) 6ns (c) 14ns

(b) 12ns (d) 18ns

Sol:- Astable Multivibrator, square wave generator.

$$T = 2 N t_{pd}$$

$$= 2 \times 3 \times 2 \text{nsec} = 12 \text{nSec}.$$



Thus time period at x and y is same.

AND GATE :-

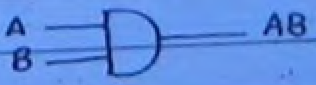
A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1

⇒ o/p is low if any of the i/p is low i.e logic '0'.

⇒ AND gate follow both commutative law and associative law.

(·) AB = BA.

i.e.



or,

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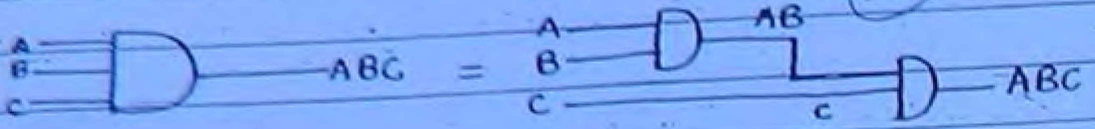
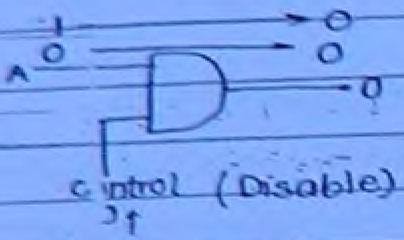
(·) $ABC = (AB)\cdot C = A(BC)$

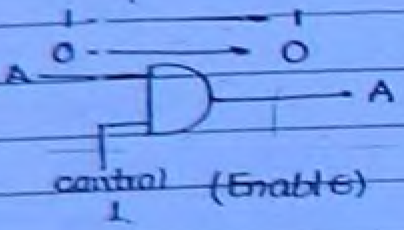
i.e.



⇒ Disable & Enables :-



⇒ Thus o/p remains in '0' due to control I/P disable. AND gate is not in working state.



⇒ AND gate is in working state o/p is changing in Enabled state.

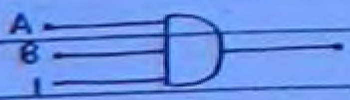
⇒ In TTL logic family, If any I/P is open and float then it will act as '1'.

⇒ In ECl logic family, floating input will act as logic '0'.

* Question occurs mostly from ECL and TTL in Exam.

Unused I/P's :-

1.

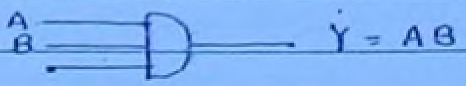


⇒ In Multipin (I/P) AND gate unused I/P can be connected to logic 1. or "pull ~~off~~ up".

⇒ unused I/P can be connected to logic '0' or "pull Down".

2. 

⇒ unused I/P can be connected to one of the used I/P.

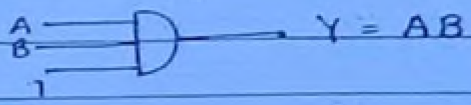
3. 

(only for TTL)

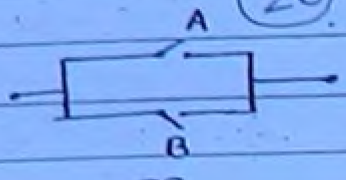
⇒ If it is TTL logic family, then unused I/P can be open or floted. (unconnected)

Note:- Because of unnecessary I/P attached to B, fan in will be down.

⇒ Best way to connecting unused pin (I/P) in AND gate is connecting to logic '1'.



OR Gate :- (Inclusive OR)



OR

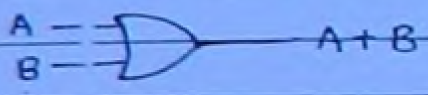
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

⇒ when any of the I/P is High in OR gate then o/p is High.

⇒ OR gate follows both commutative and Associative law.

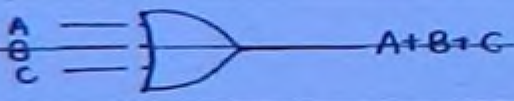
(i) commutative law :-

$A+B = B+A$

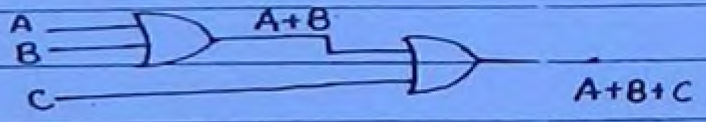


(ii) Associative law :-

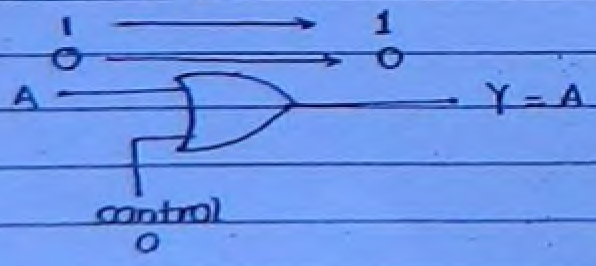
$A+B+C = (A+B)+C = A+(B+C)$



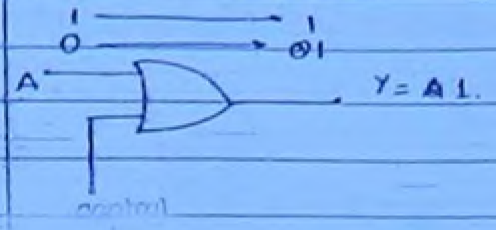
=



⇒ Enable and Disable :-



⇒ o/p is changing as I/p is changing or we say the gate is enabled.



⇒ O/P is fixed or not changed. it is said to be disable.

Unused I/P's :-

1. In OR gate, unused I/P is connected to logic '0' - "pull down."

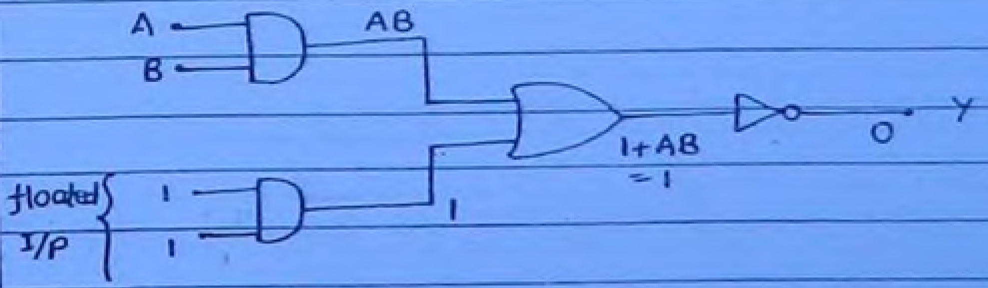
2. Connect to one of the used I/P.

3. If it is ECL then unused I/P can be open or floated.

⇒ In OR gate, Best way of connecting the unused I/P is ~~d~~ to connect to logic '0'.

Gate-2004.

Problem:- In the ckt shown in fig. in TTL, AND, OR, INVERTER ckt for the given I/P O/P is



[✓ (a)] 0

(b) 1

(c) AB

(d) $\overline{AB}$

Sol:- In TTL, all I/P's are float then it is logic 1

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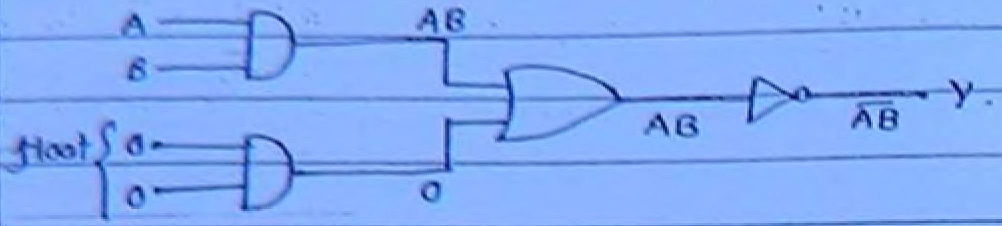
Problem For ECL AND, OR, INVERTER.

(26)



(A) 0

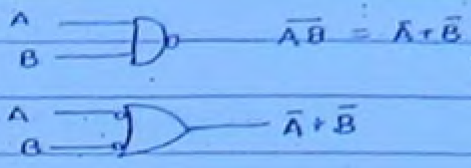
(B) 1

(C) AB

(D) $\overline{AB}$

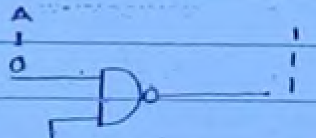
Sol:- If all I/p are floating in ECL then it is '0' and O/p $Y = \overline{AB}$ Ans$_C$

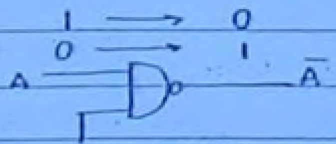
NAND GATE :- (Bubbled OR)



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

⇒ When both I/p high the O/p is low.

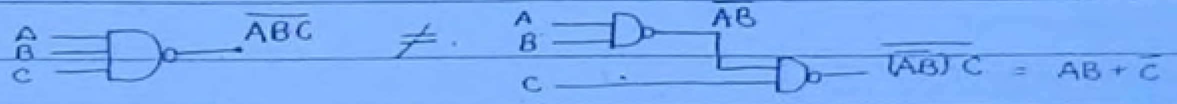




0 disable (notchanging if one I/p is zero)

1 enable.

⇒ NAND gate follow commutative law but not follow associative l



⇒ The only two gate not follow associative law i.e universal gate NAND or NOR gate.

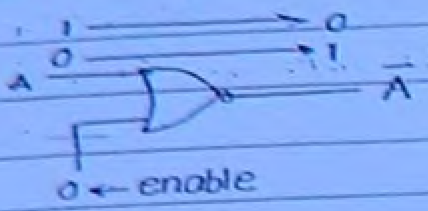
⇒ Unused I/p in NAND gate can be connected similar to unused I/p in AND gate

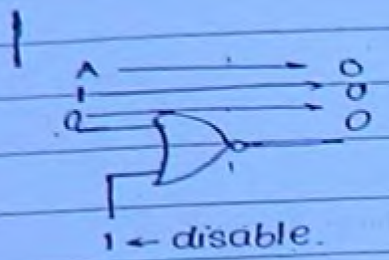
NOR GATE :- (Bubbled AND)

⇒ OR gate followed by NOT gate.

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

⇒ when both I/P is low the o/p is High.





⇒ enable and disable both are same as OR gate.

⇒ NOR gate follow commutative law and not follow associative law.

i.e. (i) $\overline{A+B} = \overline{B+A}$

(ii) $\overline{A+B+C} \neq \overline{\overline{A+B}\ C}$

⇒ unused I/P in NOR Gate can be connected similar to OR gate.

EXOR or, XOR :-

⇒ Exclusive OR gate.

⇒ OR gate is also called as inclusive OR gate.

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0

⇒ when A = B, o/p is low i.e '0'.

⇒ when A≠B, o/p is High i.e. logic '1'.

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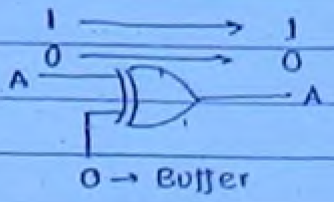
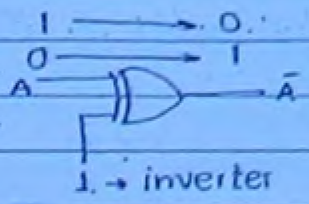




⇒ It is also called controlled inverter.

Note :- $A \oplus A = 0$

$A \oplus \bar{A} = 1$

$A \oplus 0 = A$

$A \oplus 1 = \bar{A}$

⇒ If $A \oplus B = C$ then.

(·) $A \oplus C = B$

(·) $B \oplus C = A$

(·) $A \oplus B \oplus C = 0$

⇒ Since, $A \oplus A = 0$

$A \oplus A \oplus A = A$

$A \oplus A \oplus A \oplus A = 0$

and so on ---

} Then we say. odd no. of same I/P gives same O/P and even no. same I/P gives ze as O/P.

⇒ $B \oplus B \oplus B \oplus ---- n = B$, if n is odd

$= 0$, if n is even.

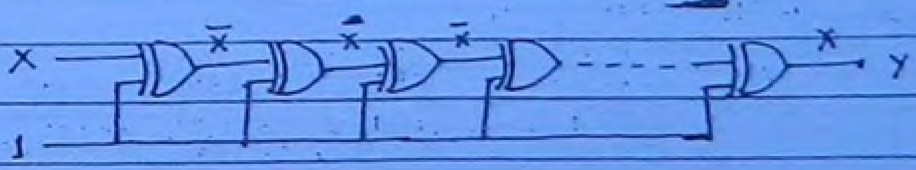
Problem :- The ckt shown in fig. contains cascading of 20 EXOR gate. If x is the I/P then O/P is.

(a) 0

(b) 1

[✓ (c) x]

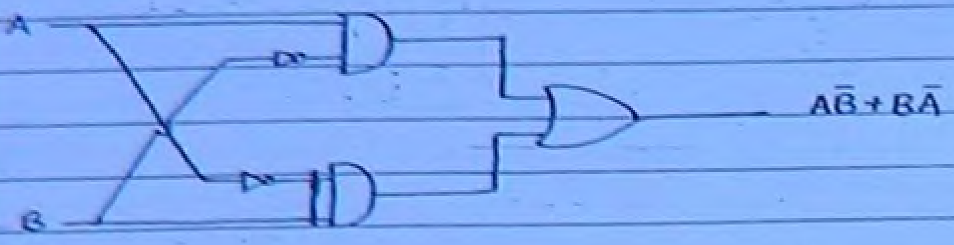
(d) $\bar{x}$



Sol: O/P of even EXOR gate have same O/P.

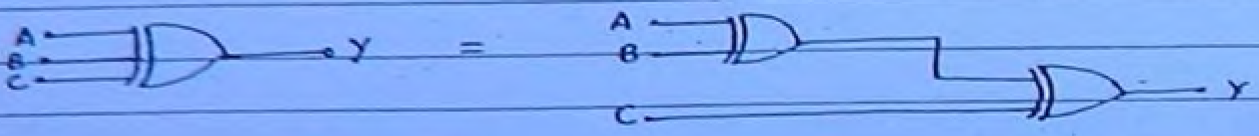
$= X$ Ans c.

Internal Diagram of EXOR gate :-



⇒ EXOR gate follow both commutative and associative law.

⇒ EXOR gate is ~~fellow~~ available with two I/P's only.



Truth table :-

	A	B	C	Y $(A \oplus B \oplus C)$
	0	0	0	0
→	0	0	1	1
→	0	1	0	1
	0	1	1	0
→	1	0	0	1
	1	0	1	0
	1	1	0	0
→	1	1	1	1

⇒ The O/P of EXOR gate is 1. when no. of 1's at the I/P is odd no.

⇒ logical expression :-

$Y = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

$= 001 + 010 + 100 + 111$ → odd no. of 1's.

$Y = \Sigma m(1,2,4,7)$

⇒ The reduced form of this expression is,

$A \oplus B \oplus C$

classmate

EXNOR or XNOR :-

A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

⇒ Whenever the I/p is same o/p is High.

SOP expression = $\bar{A}\bar{B} + AB$

POS expression = $(A+\bar{B})(\bar{A}+B)$

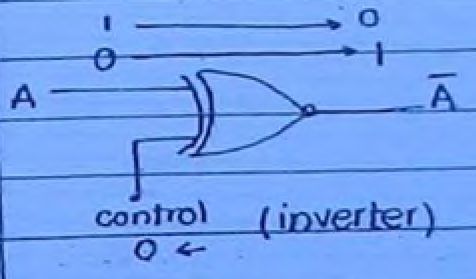
EXOR :- $\bar{A}B + A\bar{B}$ ← SOP	→ EXNOR :- $\bar{A}\bar{B} + AB$
$(A+B)(\bar{A}+\bar{B})$ ← POS	→ $(A+\bar{B})(\bar{A}+B)$

⇒ when A = B , then O/p is High. therefore coincidence logic ckt and also called as equivalent detector.

⇒ when $A \neq B$, The o/p is low.

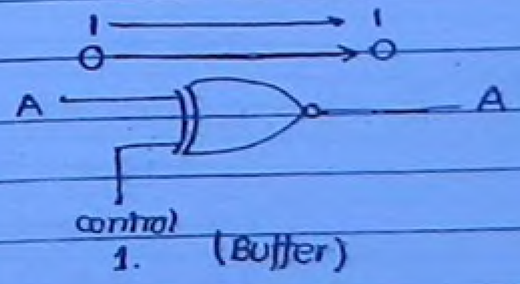
⇒ Enable and Disable :-

(i)



(inverter)

(ii)



(Buffer)

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$A \odot A = 1$

$A \odot \bar{A} = 0$

$A \odot 0 = \bar{A}$

$A \odot 1 = A$

since, $A \odot A = 1$

$A \odot A \odot A = A$

$A \odot A \odot A \odot A = 1.$

and so on.

$B \odot B \odot B \odot ---- n = 1$, if n = even

B if n = odd.

⇒ EXOR and EXNOR is not always complement, it is complement only when the no. of I/P is even. and if I/P is odd then EXOR and EXNOR are same.

i.e. $A \oplus B \oplus C = A \odot B \odot C$ ⇒ same.

and, $A \oplus B \oplus C \oplus D = \overline{A \odot B \odot C \odot D}$ ⇒ complement

Ques:- Find expression of $A \odot B \odot C$.

Sol:- $A \odot B \odot C$

$= (\bar{A}\bar{B} + AB) \odot C$

$= \overline{(\bar{A}\bar{B} + AB)}\,\bar{C} + (\bar{A}\bar{B} + AB)C$

$= (\overline{\bar{A}\bar{B}} \cdot \overline{AB})\bar{C} + (\bar{A}\bar{B} + AB)C$

Since, $\overline{(\bar{A}B + AB)} = (\overline{A \odot B}) = A \oplus B. = \bar{A}B + A\bar{B}$

$= (\bar{A}B + A\bar{B})\bar{C} + (\bar{A}\bar{B} + AB)C$

$= \bar{A}B\bar{C} + A\bar{B}\bar{C} + \bar{A}\bar{B}C + ABC$

$= A \oplus B \oplus C.$

JTO-2009

Ques:- Minimize.

	A	B	C	Y
→	0	0	0	1
	0	0	1	0
	0	1	0	0
→	0	1	1	1
	1	0	0	0
→	1	0	1	1
→	1	1	0	1
	1	1	1	0

(A) $A \oplus B \oplus C$

(B) $A \odot B \odot C$

✓(C) $\overline{A \odot B \odot C}$

(D) $AB + BC + AC$

Sol:- for EXOR → O/P is 1 when odd no. of 1's at I/P.

In this case.,

$$Y = \overline{A \oplus B \oplus C}$$

$$= \overline{A}\,\overline{\odot B \odot C}$$ Ans C.

⇒ EXOR and EXNOR are never always complemented, It is complement only when even variable occurs.

⇒ EXNOR gate is even no. of 1's detector when no. of I/P's are even.

⇒ EXNOR gate is odd no. of 1's detector when no. of I/P's are odd.

Problem:- $\bar{A} \oplus B = A \odot B$.

Sol:- Put $X = \bar{A}$, $Y = B$

$X \oplus Y$

$= ~~A~~\; X\bar{Y} + \bar{X}Y$

$= \bar{A}\bar{B} + AB = A \odot B$.

Problem:- $\bar{A} \oplus \bar{B}$

Sol:- Put $X = A$, $Y = \bar{B}$

$= X \oplus Y$

$= X\bar{Y} + Y\bar{X}$

$= AB + \bar{A}\bar{B}$

$= A \odot B$.

Problem- $A \oplus B \oplus AB.$

Sol:- $(A\bar{B}+\bar{A}B) \oplus AB$

$= (A\bar{B}+\bar{A}B)\overline{AB} + \overline{(A\bar{B}+\bar{A}B)}AB$

$= A\bar{B}(\bar{A}+\bar{B}) + \bar{A}B(\bar{A}+\bar{B}) + (\overline{A\bar{B}} \cdot \overline{\bar{A}B})AB$

$= A\bar{B} + \bar{A}B + [(\bar{A}+B)(A+\bar{B})]AB$

$= A\bar{B} + \bar{A}B + [\bar{A}\bar{B} + AB]AB$

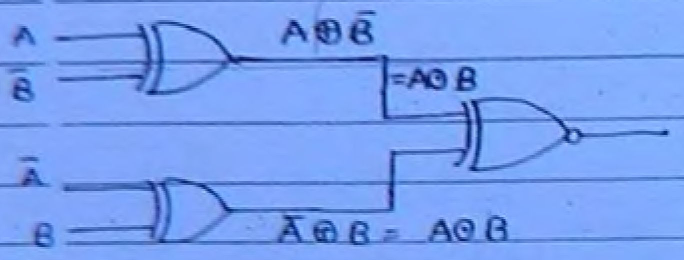
$= A\bar{B} + \bar{A}B + AB$

$= A(\bar{B}+B) + \bar{A}B = A + \bar{A}B$

$= (A+\bar{A})(A+B) = A+B$ Ans_c

$$\boxed{A \oplus B \oplus AB = A+B}$$

Problem:-



$\because X \odot X = 1$

$A \odot Y$ $Y = 1.$

(a) 0

(b) 1

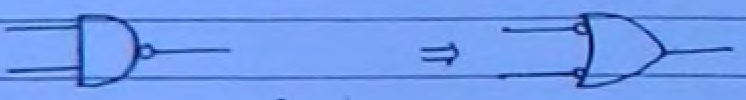
(c) $A \oplus B$

(d) $A \odot B$

Sol:- $Y = 1$ Ans_c

SYMBOLS :-

NAND ⇒

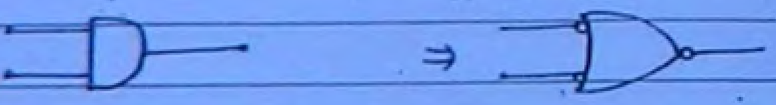


Bubbled OR

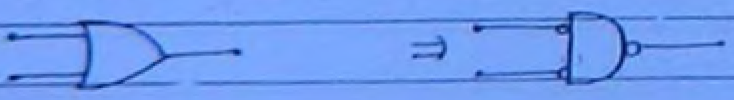
NOR ⇒

Bubbled AND.

AND ⇒



OR ⇒

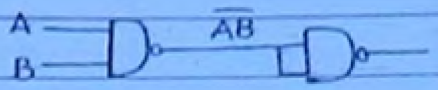


NAND as Universal :-

(i) NOT :-

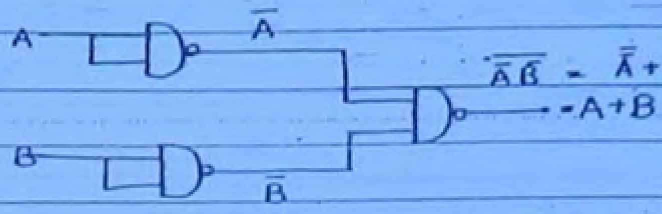
⇒ 1 gate required

(ii) AND :-



⇒ 2 gate

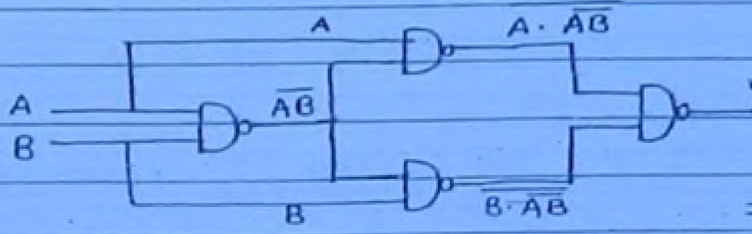
(iii) OR :-



$\overline{\bar{A}\bar{B}} = \bar{\bar{A}} + \bar{\bar{B}}$ ⇒ 3 gate.

= A+B

(iv) EXOR :-

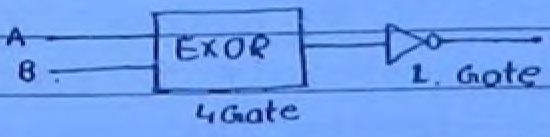


$Y = A \oplus B = \bar{A}B + A\bar{B}$

⇒ 4 Gate.

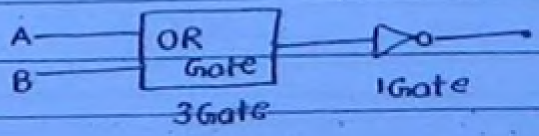
$$Y = \left(\overline{\overline{A\cdot\overline{AB}} \cdot \overline{B\cdot\overline{AB}}}\right)$$
$$= \left(A\cdot\overline{AB} + B\cdot\overline{AB}\right)$$
$$= \left(A(\bar{A}+\bar{B}) + B(\bar{A}+\bar{B})\right)$$
$$= A\bar{B} + B\bar{A} = A \oplus B$$

(v) EXNOR :-



⇒ 5 Gate

(vi) NOR :-



⇒ 4 Gate

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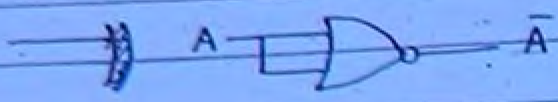
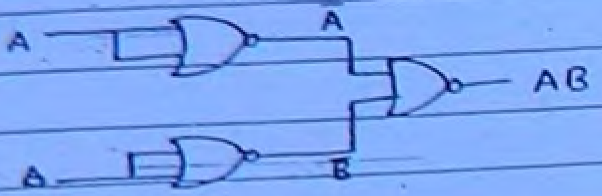
NOR AS universal :-

(i) NOT :-



⇒ 1 gate

(ii) AND :-

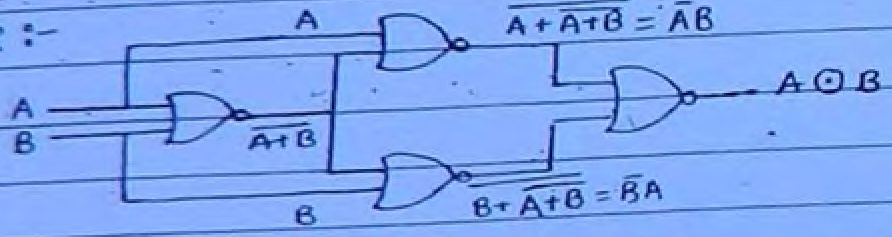


⇒ 3 gate

(iii) OR :-

⇒ 2 gate

(iv) EXNOR :-



⇒ 4 gate

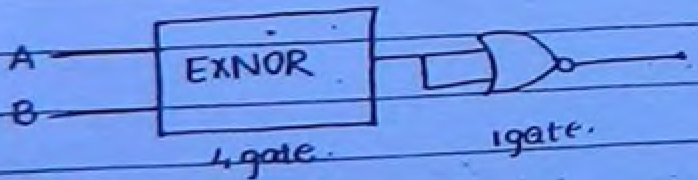
$$y = \overline{(\overline{A+\overline{A+B}}) + (\overline{B+\overline{A+B}})} = \overline{\bar{A}(A+B) + \bar{B}(A+B)}$$

$$= \bar{A}B + \bar{B}A = \overline{A\oplus B}$$

~~$= (A \cdot \overline{A+B})(B+\overline{A+B})$~~

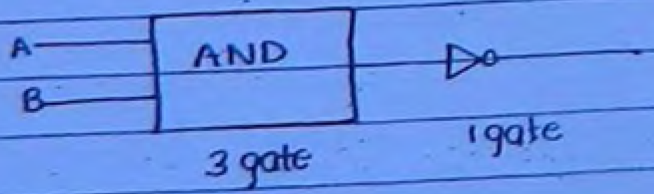
~~$= AB + A(\bar{A}\bar{B}) + B(\bar{A}\bar{B}) + AB$~~ $= A \odot B$

(v) EXOR :-



EXOR ⇒ 5gate

(vi) NAND



NAND ⇒ 4 gate

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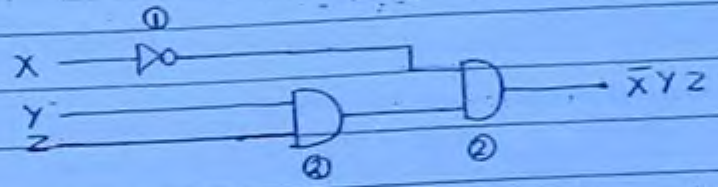
Note:-

logic gate	No. of NAND	No. of NOR.
NOT	1	1
AND	2	3
OR	3	2
EXOR	4	5
EXNOR	5	4.

Problem:- To implement $\bar{X}YZ$. The min no. of two I/P NAND gate required.

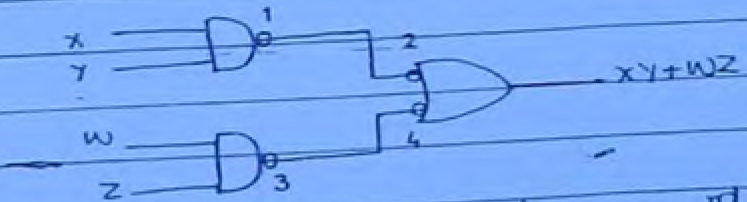
Sol:-



Total no. of NAND gate = 2+2+1 = 5. Ans.

Problem:- To implement XY + WZ, the min no. of 2 input NAND gate required.

Sol:-



⇒ 1st inverter cancelled 2nd and 3rd cancelled 4th.

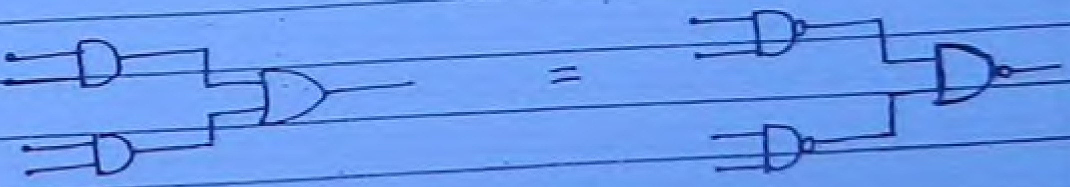
⇒ Now the total no. of NAND gate is

= 2 + Bubbled OR (= NAND)

= 2 + 1 = 3.

= 3 NAND gate required.

Note:-



Two level AND-OR = Two level NAND-NAND

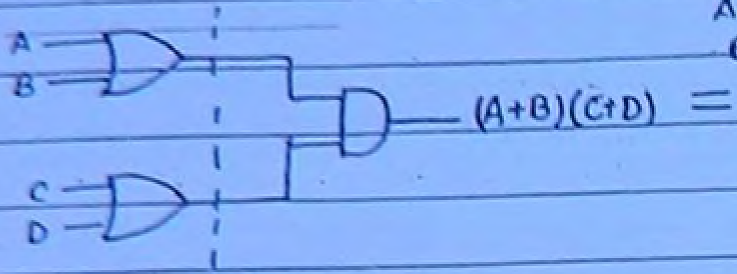
$$\boxed{\text{AND-OR} = \text{NAND-NAND}}$$

⇒ To implement SOP form, only NAND gate alone.

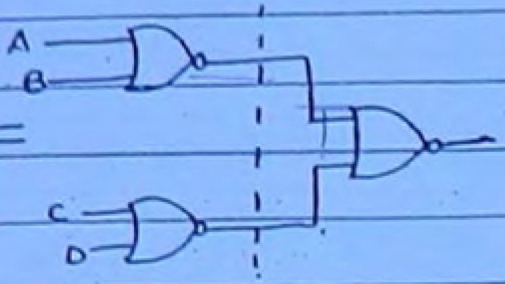
⇒ To implement POS form, only NOR gate alone.

Q:- if (A+B)(C+D). then min no. of Gate.

Sol:-



Two level OR - AND



Two level NOR - NOR.

⇒ $\boxed{\text{OR- AND = NOR - NOR}}$

Digital circuits

combination ckt	Sequential ckt
⇒ Present O/P is only depend on present I/P.	⇒ Present O/p → Present I/p └→ Previous O/p
⇒ No feedback	⇒ feedback.
⇒ No memory	⇒ Memory.
⇒ e.g. Half Adder (HA) FA MUX DEMUX	⇒ eg:- FlipFlop (FF) Register Counter.

COMBINATIONAL CIRCUIT

Procedure to Design :-

- (-) Identify I/P and O/P.
- (-) Construct truth table
- (-) Write logical expression in SOP or POS form.
- (-) Minimize logical expression if possible
- (-) Implement logic circuits.

(A) HALF ADDER (HA) :-

(i)

(ii) Truth table :-

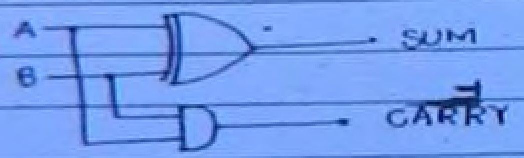
A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

(iii) logical expression :-

SUM = $\bar{A}B + A\bar{B}$ = $A \oplus B$

CARRY = AB.

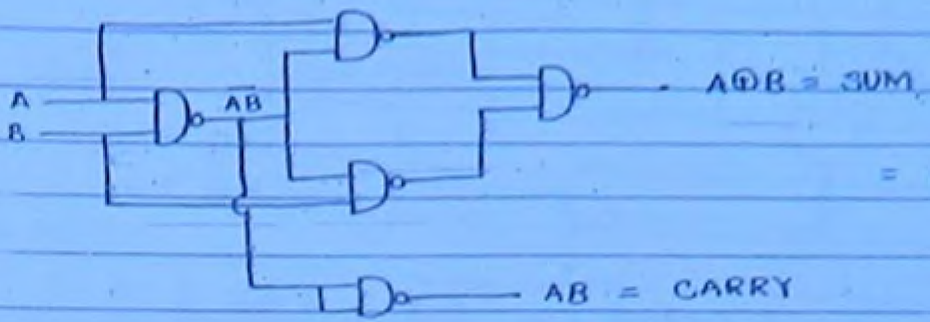
(iv) Implement :-



Important Ques :-

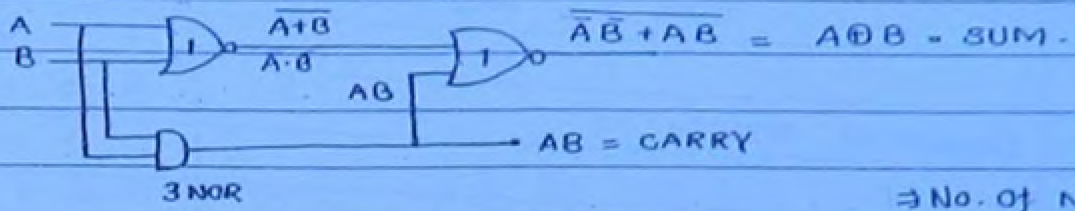
- (-) logical Expression for SUM :- $A \oplus B$ CARRY : AB
- (-) Min. no. of NAND Gate : 5
- (-) Min no. of NOR Gate : 5
- (-) no. of MUX : 3
- (-) no. of DECODER : 1, 2x4 Decoder and 1 OR Gate

HA using NAND gate :-



= no. of gate = 5.

HA using NOR Gate :-

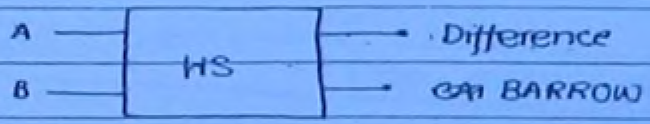


⇒ No. of NOR gate !

Total no. of gate = 2+3 = 5.

(B) HALF SUBTRACTOR :-

(i)



(ii) Truth table :-

A	B	Diff	Barrow
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

(iii) logical expression :-

Difference = $\bar{A}B + A\bar{B}$

BARROW = $\bar{A}B$

(iv) Implement :-

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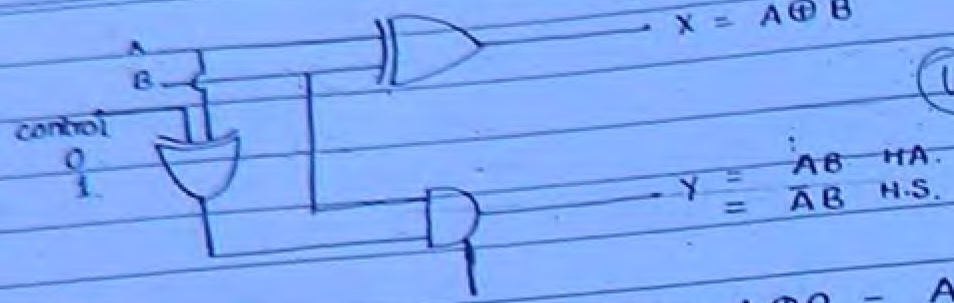
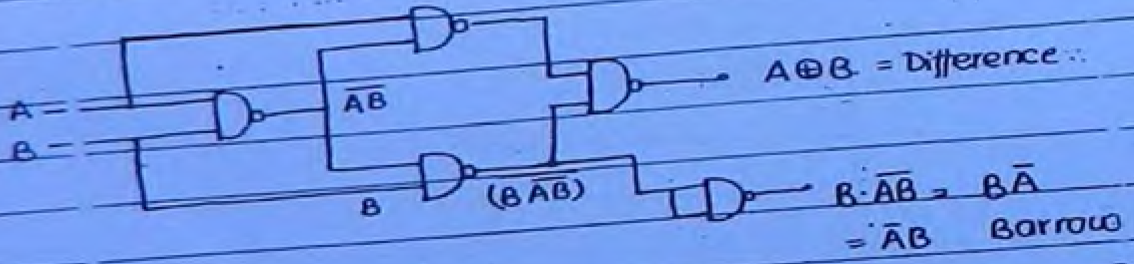


Note :- (i) if control = 0 then A ⊕ 0 = A
then Y = AB and ckt is HA.
(ii) if control = 1 then, A ⊕ 1 = Ā
then Y = ĀB and ckt is HS.

Importa nt Ques :-

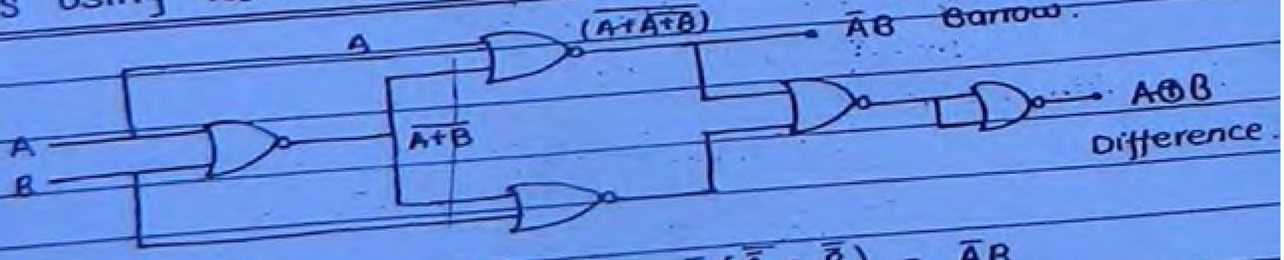
No. of NAND Gate = 5
No. of NOR Gate = 5
No. of MUX :- 3 . (2x1 MUX)
No. of DECODER :- 1 (2x4) Decoder and 1 OR Gate.
logica expression for Difference = $A\bar{B} + \bar{A}B$, Barrow : $\bar{A}B$.

HS using NAND gate :-



No. of NAND Gate = 5

HS using NOR Gate :-



Now, $\overline{A+\overline{\bar{A}\cdot\bar{B}}} = \bar{A}(\bar{A}\cdot\bar{B}) = \bar{A}(\bar{A}+\bar{B}) = \bar{A}B$

⇒ No of NOR gate = 5

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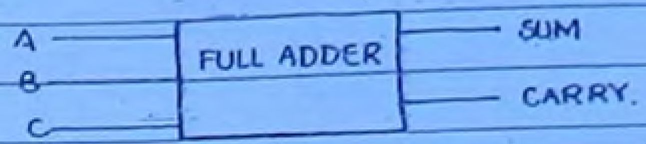
(C) FULL ADDER :-

(i)



(ii) Truth table:-

A	B	C	SUM	CARRY
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(iii) logical expression :-

$$SUM = \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC = A \oplus B \oplus C$$

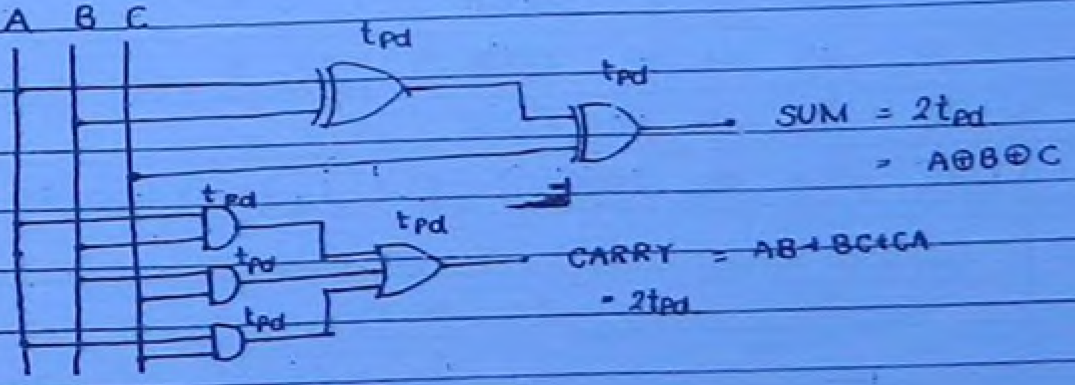
$$= \Sigma m(1,2,4,7)$$

$$CARRY = \bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$$

$$= AB + BC + AC.$$

⇒ The truth table of carry shows the majority of 1's function.

$$= \Sigma m(3,5,6,7)$$



⇒ In full adder each logic gate have propogation delay of t_{pd} to provid sum or carry o/p, it requires to $2t_{pd}$ delay.

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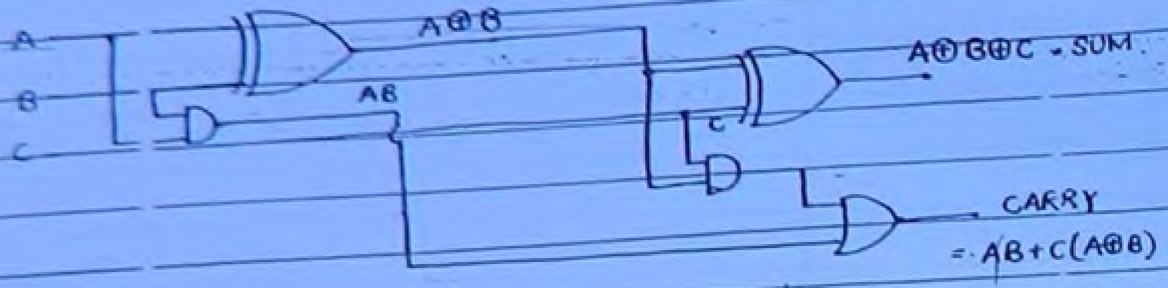
Now, CARRY ~~SUM~~ = $\bar{A}BC + A\bar{B}C + AB\bar{C} + ABC$

$= AB(C+\bar{C}) + C(\bar{A}B + A\bar{B})$

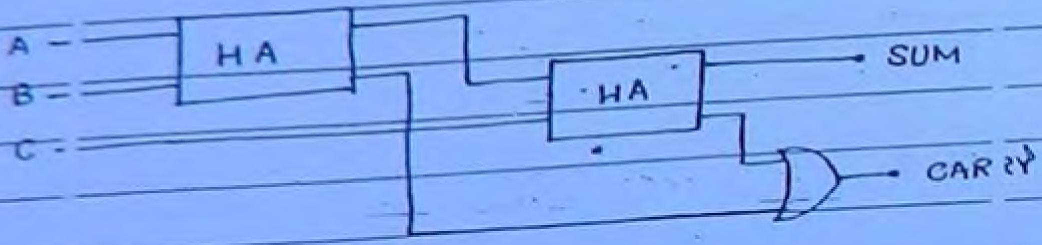
$= AB + C(A \oplus B)$ —(ii)

$$\boxed{CARRY = AB + C(A \oplus B)}$$

Implementation:-



i.e.



Important ques:-

(i) logical expression for SUM = $A \oplus B \oplus C$ CARRY = $AB+BC+AC$

(ii) No. of HA and OR gate = 2HA, 1-OR

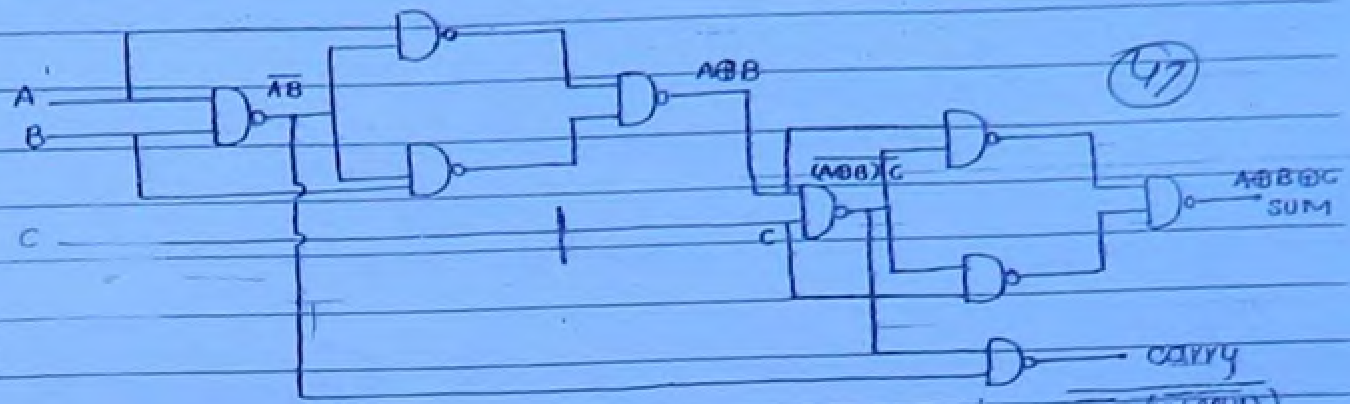
(iii) Min. no. of NAND = 9

(iv) min. no. of NOR = 9

(v) No. of MUX =

(vi) No. of DECODER = 1, (3×8) Decoder and 2-OR gate

(i) Implementation of Full adder using NAND gate :-

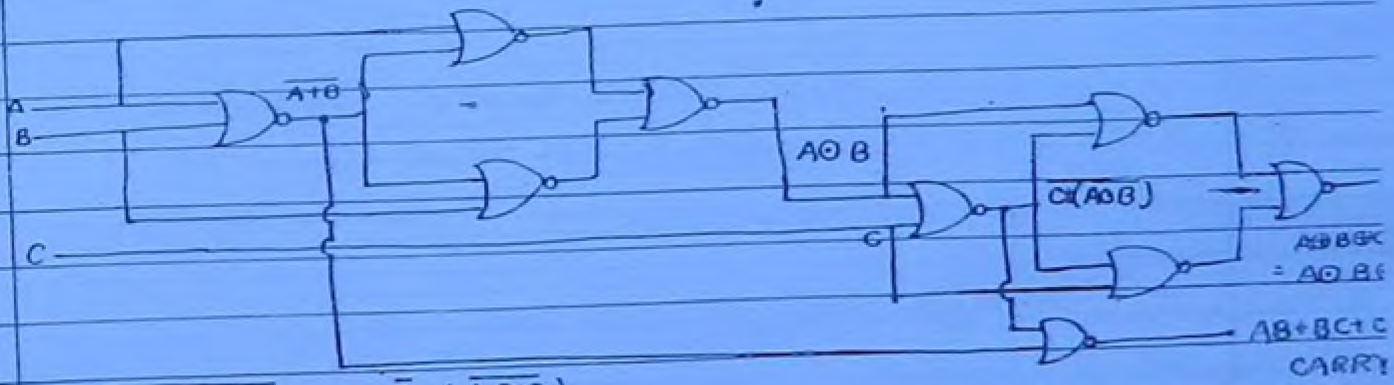


$$\overline{\overline{AB}\cdot\overline{(C(A\oplus B))}}$$

$$= AB + C(A\oplus B)$$

(ii) Implementation of Full adder using NOR Gate :-

Since $A\oplus B\oplus C = A\odot B\odot C$. The the ckt is same only NAND is replaced by NOR.



$$\overline{C+(A\ominus B)} = \bar{C}\cdot(\overline{A\odot B})$$

and,

$$\overline{\overline{A+B} + \bar{C}\cdot(\overline{A\odot B})} = \overline{\overline{(A+B)}}\cdot\bar{\bar{C}}(A\oplus B)$$

$$= (A+B)(C+\overline{A\oplus B})$$

$$= AC + A\bar{A}\bar{B} + AAB + BC + B\bar{A}\bar{B} + BAB$$

$$= AC + AB + BC + AB$$

$$= C(A+B) + AB$$

CARRY $= AB + BC + CA$

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48

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PARALLEL ADDER :-

There are three type of adder

1. Serial adder (we write with sequential ckt)
2. Parallel adder.
3. look ahead carry adder.

⇒ In serial adder only one Full adder (FA) is used to add grou of bits.

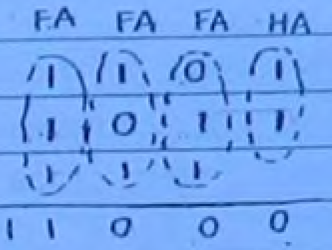
⇒ It is slowest adder.

Parallel adder :-

⇒ For 4 bit adder

:- 3 FA and 1 HA required.

:- or 4 FA is required.



⇒ Parallel adder is used to add group of bits.

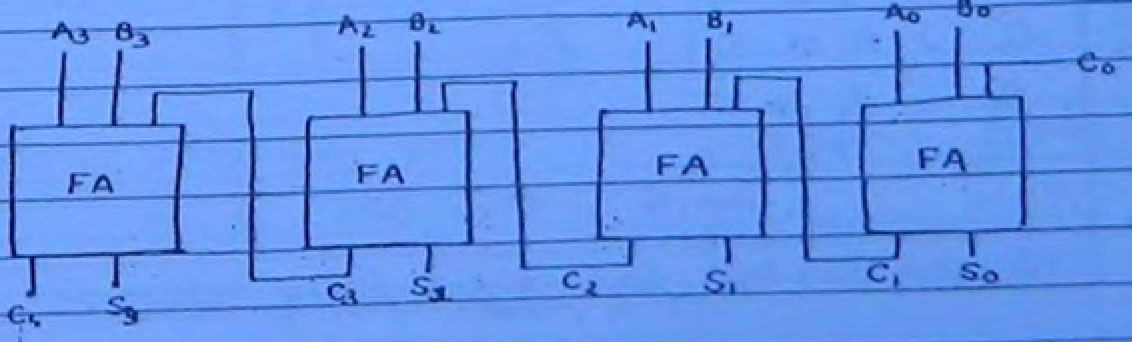
⇒ To add two N bit no. it requires (N-1) Full adder and 1 Half adder. or,

N Full adder or,

(2N-1) Half adder and (N-1) OR gates required.

Now.

Diagram of Parallel adder :-



A_3	A_2	A_1	A_0
1	1	0	1
1	0	1	1
B_3	B_2	B_1	B_0

$\underbrace{C_4}_{\text{CARRY}}$ $\underbrace{S_3\ S_2\ S_1\ S_0}_{\text{SUM}}$

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⇒ Parallel adder is also called Ripple carry adder.

⇒ Propogation delay from I/P array to O/P array. Hence it is also known as Ripple carry adder.

⇒ In parallel adder each FA will provide 2 logic gate delay In n bit parallel adder provide total delay of.

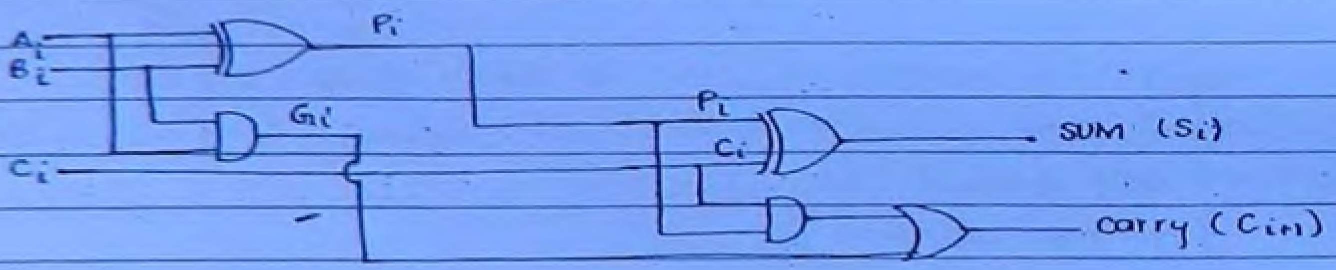
$$\boxed{T_{delay} = 2n t_{pd}}$$

LOOK AHEAD CARRY CIRCUIT :-

⇒ Disadvantage of parallel adder is carry propogation delay present.

⇒ As no.of bit increases - speed of operation reduced.

⇒ To avoid this look ahead carry adder is used.



P_i = Propogation

G_i = Generation term

$P_i = A_i \oplus B_i$

$G_i = A_i \cdot B_i = A_i B_i$

$S_i = P_i \oplus C_i$

$C_{i+1} = P_i C_i + G_i$

For four (4) bit look ahead carry adder :-

I/P. A_3 A_2 A_1 A_0

B_3 B_2 B_1 B_0

Then $P_0 = A_0 \oplus B_0$

$P_1 = A_1 \oplus B_1$

$P_2 = A_2 \oplus B_2$

$P_3 = A_3 \oplus B_3$

$G_0 = A_0B_0$ $S_0 = P_0 \oplus C_0$

$G_1 = A_1B_1$ $S_1 = P_1 \oplus C_1$

$G_2 = A_2B_2$ $S_2 = P_2 \oplus C_2$

$G_3 = A_3B_3$ $S_3 = P_3 \oplus C_3$

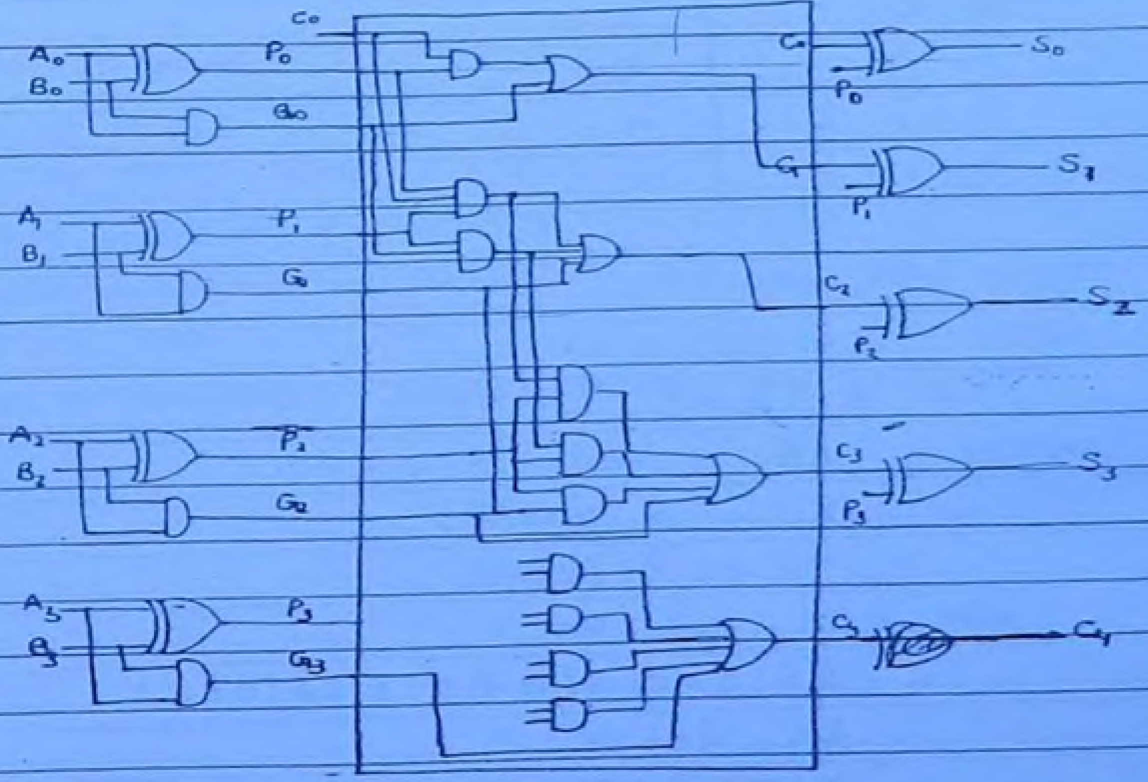
$$\boxed{C_{i+1} = P_iC_i + G_i}$$ look ahead carry generator expression.

$C_1 = P_0C_0 + G_0$

$C_2 = P_1C_1 + G_1 = P_1(P_0C_0 + G_0) + G_1 = P_1P_0C_0 + P_1G_0 + G_1$

$C_3 = P_2C_2 + G_2 = P_2P_1P_0C_0 + P_2P_1G_0 + P_2G_1 + G_2$

$C_4 = P_3C_3 + G_3 = P_3P_2P_1P_1C_0 + P_3P_2P_1G_0 + P_3P_2G_1 + P_3G_2 + G_3.$



⇒ Total no. of AND Gate inside $= 1+2+3+4 = \frac{n(n+1)}{2} = \frac{4 \times 5}{2}$

no. of AND Gate $= \frac{n(n+1)}{2}.$

no. of OR Gate $= n.$

⇒ Total propogation delay $= 2t_{pd}.$

⇒ This is faster than parallel adder.

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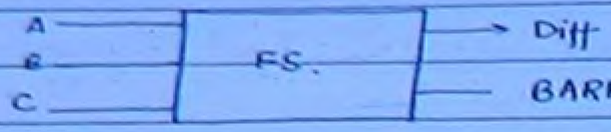
FULL SUBTRACTOR :-

(i)



(ii) Truth table :-

A	B	C	Diff (A-B-C)	BARROW
0	0	0	0	0
0	0	1	1	1
^{2}0	1	0	1	1
^{2}0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

(iii) logic expression :-

Diff :- $\Sigma m\ (1, 2, 4, 7)$

$= A \oplus B \oplus C$

BARROW $= \bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}BC + ABC$

$= BC + \bar{A}\ (\bar{B}C + B\bar{C})$

$= BC + \bar{A}\ (B \oplus C)$

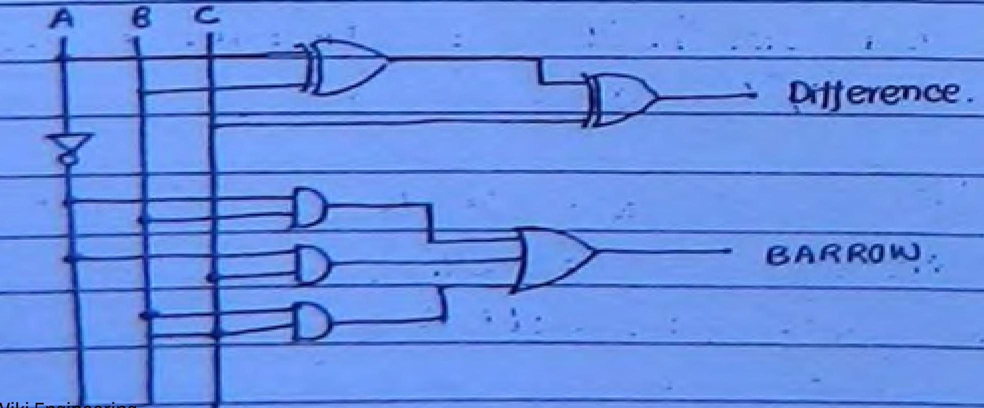
add $\bar{A}BC$ two more :-

$= \bar{A}B(\bar{C} + C) + (\bar{A} + A)BC + C\bar{A}\ (B + \bar{B})$

$= \bar{A}B + \bar{A}C + BC$

$= \Sigma m\ (1, 2, 3, 7)$

(iv) Implementation :-

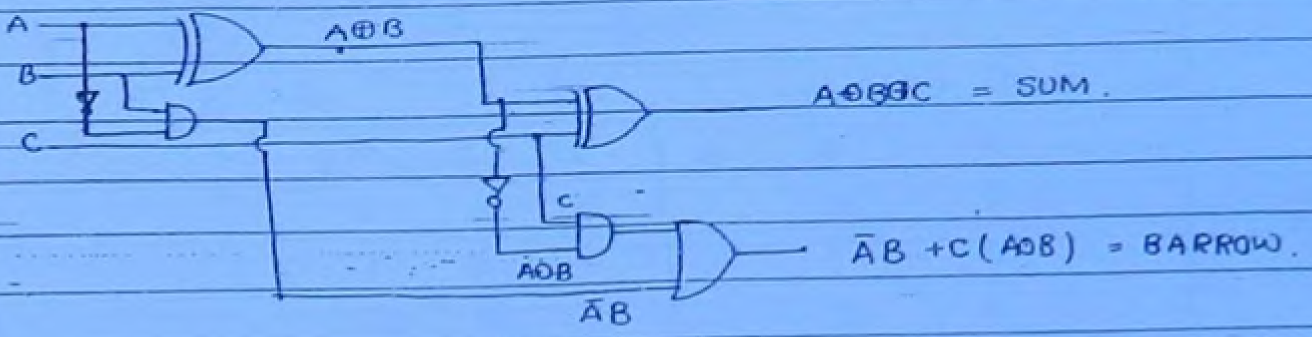


Barrow expression :-

$$\bar{A}\bar{B}C + \bar{A}B\bar{C} + \bar{A}B\bar{\bar{C}} + ABC$$

$$= \bar{A}B(C+\bar{C}) + C(\bar{A}\bar{B} + AB)$$

$$= \bar{A}B + C(A \odot B)$$



⇒ Full subtractor will be implemented with 2-HS and 1 OR Gate.

Important ques :-

no. of NAND gate = 9

no. of NOR gate = 9

logical expression for Difference = $A \oplus B \oplus C$

logical expression for Barrow = $\bar{A}B + \bar{A}C + BC$ or, $\bar{A}B + C(A \odot B)$

no. of MUX :-

no. of Decoder :- 1 (3x8) Decoder and 2 OR gate

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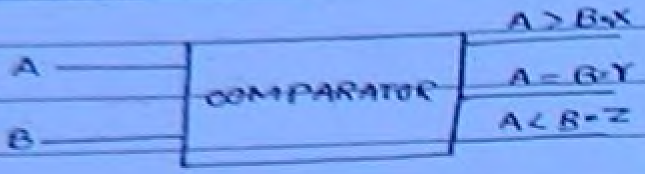
COMPARATOR :-

(i)



(ii) Truth table :-

A	B	G	X	Y	Z
0	0		0	1	0
0	1		0	0	1
1	0		1	0	0
1	1		0	1	0

$X = A\bar{B}$ $\quad Y = A \odot B$ $\quad Z = \bar{A}B$

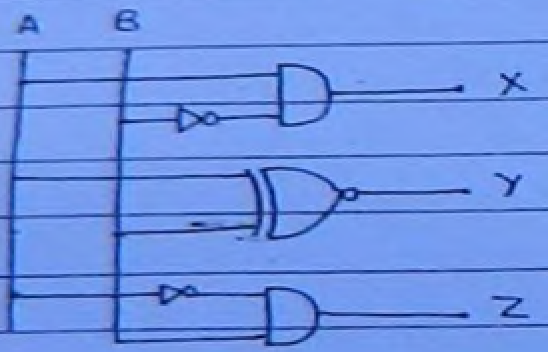
(iii) Expression :-

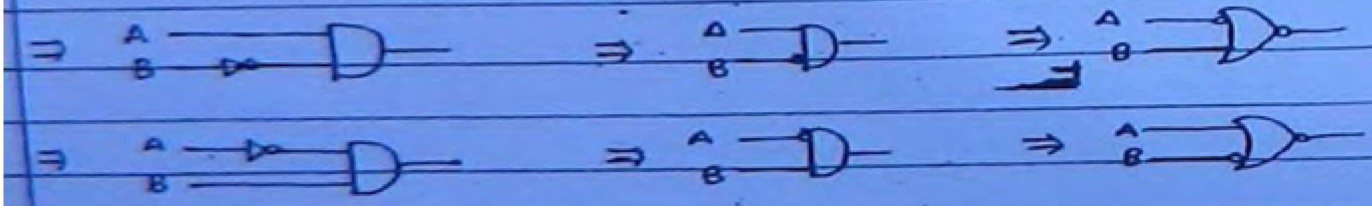
$X = A\bar{B}$

$Y = A \odot B = \bar{A}\bar{B} + AB$

$Z = \bar{A}B$

(iv) Implementation :-





⇒ Note:-for equality condition $A \odot B$. condition Holds.

⇒ If $A_3 A_2 A_1 A_1$ are equal to $B_3 B_2 B_1 B_0$

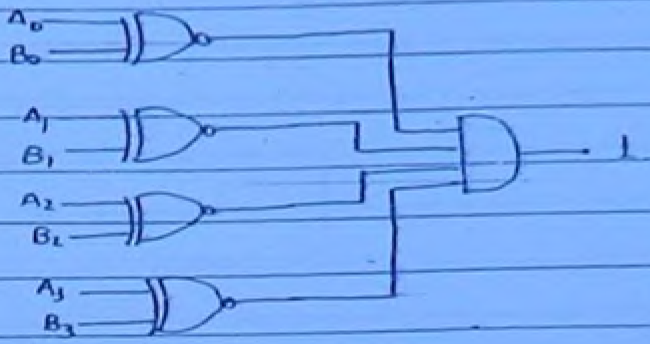
Then the equality condition is.

$(A_3 \odot B_3)\ (A_2 \odot B_2)\ (A_1 \odot B_1)(A_0 \odot B_1)$

alternate

DATE

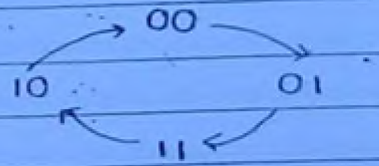
Then the ckt is :-



K - MAP :-

- ⇒ It is used when o/p is 0, 1, and X (don't care)
- ⇒ In K-MAP gray code representation is used
- ⇒ K-map is graphical representation

⇒ Gray code representation



⇒ each successive term is changed by only one bit.

Two variable :-

MSB A \ LSB B	0	1
0	0 00	1 01
1	2 10	3 11

(For Two variable)

For Three variable :-

MSB A \ LSB BC	00	01	11	10
0	0 00	1 01	3 11	2 10
1	4	5	7	6

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56

four variable:-

AB \ CD	00	01	11	10
00	0	1	3	2
01	4	5	7	6
11	12	13	15	14
10	8	9	11	10

⇒ Minimize :-

Q:- $f(A,B) = \Sigma m(0,2,3)$

Sol:-

A \ B	0	1
0	1	
1	1	1

$f(A,B) = A + \bar{B}$ (+ is put due to SOP form)

Q: $f(A,B) = \Sigma m(1,2,3)$

Sol:-

A \ B	0	1
0		1
1	1	1

$f(A,B) = A + B$

Q:- $f(A,B) = \Sigma m(0,1,2,3)$

Sol:- $f(A,B = 1$.

⇒ In K-map if all are one means the function is 1.

Q:- ~~f(A,B)~~ $= \Sigma m(1,3) + \Sigma d(2)$

Sol:-

A \ B		
		1
	X	1

$f(A,B) = B$ (no need of any gate)

Q:- $f(A,B) = \Sigma m(0,3) + \Sigma d(2)$

Sol:-

A\B	0	1
0	1	
1	1	*

$f(A,B) = A + \bar{B}$

Q:- $f(A,B) = \Sigma(0,3) + \Sigma d(2,1)$

Sol:-

A\B		
	1	*
	*	1

$f(A,B) = 1.$

⇒ In SOP form if all are 1's means o/p is 1.

⇒ All are don't care means dont care.

Three variable :-

Q:- $f(A,B,C) = \Sigma m(1,3,5,7)$ -

Sol:-

A\BC	00	01	11	10
0		1	1	
1		1	1	

$f(A,B,C) = C.$

Q:- $f(A,B,C) = \Sigma m(0,1,3,6)$

Sol:-

A\BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	1	
A				1

$f(A,B,C) = \bar{A}\bar{B} + \bar{A}C + AB\bar{C}$

Q:- $f(A,B,C) = \Sigma m(1,3,6,7)$

Sol:-

A\BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1	1	
A			1	1

⇒ if we take BC then it is redundant term and it must be removed.

PAGE

alternate $f(A,B,C) = \bar{A}C + AB$

Procedure :-

(i) Octets
(ii) Quads
(iii) Pairs
(iv) Single term
(v) Remove redundant

↓ Priority.

Q :- $f(A,B,C) = \Sigma m(0,1,2,4,7)$

Sol :-

$A \backslash BC$	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1		1
A	1		1	

$= \bar{A}\bar{B} + \bar{A}\bar{C} + \bar{B}\bar{C} + ABC$

Q :- $f(A,B,C) = \Sigma m(0,1,5,6,7)$

Sol :-

$A \backslash BC$	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1		
A		1	1	1

$f(A,B,C) = \bar{A}\bar{B} + \bar{B}C + AB$
$= \bar{A}\bar{B} + AB + AC$
} two solⁿ

⇒ K-map provide minimize expression but not neccesarly unique. ie two solⁿ also.

Q :- $f(A,B,C) = \Sigma m(0,1,2,5,7) + \Sigma d(3,6)$

Sol :-

$A \backslash BC$	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	X	1
A		1	1	X

$f(A,B,C) = \bar{A} + C$

Q :- $f(A,B,C) = \Sigma m(0,1,6,7) + \Sigma d(3,5)$

Sol:

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	X	
A		X	1	1

$f(A, B, C) = \bar{A}\bar{B} + AB$

Q: $f(A,B,C) = \Sigma m(0,1,6,7) + \Sigma d(3,4,5)$

Sol:-

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$	1	1	*	
A	*	*	1	1

$f(A,B,C) = \bar{B} + AB$

Four Variable :-

Q: $f(A,B,C,D) = \Sigma m(0,1,3,5,7,8,9,11,13,15)$

Sol:

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	
$\bar{A}B$	4	1	1	
AB		1	1	
AB	1	1	1	

$f(A,B,C,D) = D + \bar{B}\bar{C}$

Q: $f(A,B,C,D) = \Sigma m(0,1,4,5,8,9,13,15)$

Sol:

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1		
$\bar{A}B$	1	1		
AB		1	1	
$A\bar{B}$	1	1	4	

$f(A,B,CD) = \bar{A}\bar{C} + \bar{B}\bar{C} + ABD$

Q: $f(A,B,C,D) = \Sigma m(0, 2, 8, 10, 14) + \Sigma d(5, 15)$

Sol:-

AB \ CD	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1			1
$\bar{A}B$		x		
AB			x	1
$A\bar{B}$	1			1

$f(A,B,C,D) = \bar{B}\bar{D} + AC\bar{D}$

POS (Product of Sum) :-

Simplify :-

Q :- $f(A,B) = \pi M(0,2,3)$

Sol:-

A \ B	$\bar{B}$,0	$\bar{B}$, 1
0, A	0	
1 $\bar{A}$	0	0

$f(A.B) = B \cdot \bar{A}$

Q :- $f(A, B) = \pi M(0,3) + \pi d(1)$

Sol :-

A \ B	B	$\bar{B}$
A	0	x
$\bar{A}$		0

$f(A,B) = A + \bar{B} = A\bar{B}$

Q : $f(A,B,C) = \pi M(0,1,3,5,7)$

Sol :-

A \ B+C	B+C	B+$\bar{C}$	$\bar{B}$+$\bar{C}$	$\bar{B}$+C
A 0	1	1	1	
$\bar{A}$ 1		1	1	

$f(A,B,C) = \bar{C} + (A+B)$

$= \bar{C}(A+B)$

Gate- 2013

Q:- for the K-map minimize POS expression is.

Sol:-

A \ BC	B+C	B+C̄	B̄+C̄	B̄+C
A	0	x	X	1
Ā	0	1	0	X

$f(A,B,C) = (B+C)(B+\bar{C})$

⇒ The two function are same if the position of 1's are 0's are same in K-map. and if the 1's place 0 are placed and at 0's place 1's are placed then the function is complemen to each other.

⇒ Problem - 26 - page - 13

Q:- $W = R + \bar{P}Q + \bar{R}S$ $X = PQ\bar{R}\bar{S} + \bar{P}\bar{Q}\bar{R}\bar{S} + P\bar{Q}R\bar{S}$

PQ \ RS	R̄S̄	R̄S	RS	RS̄
P̄Q̄		1	1	1
P̄Q	1	1	1	1
PQ		1	1	1
PQ̄		1	1	1

PQ \ RS	R̄S̄	R̄S	RS	RS̄
P̄Q̄	1			
P̄Q				
PQ	1			
PQ̄	1			

$Y = RS + PR + P\bar{Q} + \bar{P}Q$ $Z = R + S + \overline{PQ + \bar{P}\bar{Q}\bar{R} + P\bar{Q}\bar{S}}$

PQ \ RS	R̄S̄	R̄S	RS	RS̄
P̄Q̄	0	0	0 1	0
PQ	1	1	1	1
PQ	1	1	0 1	0
PQ̄	0	0	0 1	0

PQ \ RS	R̄S̄	R̄S	RS	RS̄
P̄Q̄	0	0 1	1	1
P̄Q	1	1	1	1
PQ	0	0 1	0 1	0 1
PQ̄		1	1	1 0

⇒ Then $W = Z. = \bar{X}$

NOTE ⇒ If Truth table is :-

A	B	Y
0	0	0
0	1	1
1	0	0
1	1	C

(The method for writing the expression from Truth table).

Then.

$Y = \bar{A}\bar{B}*0 + \bar{A}B*1 + A\bar{B}*0 + AB*C$

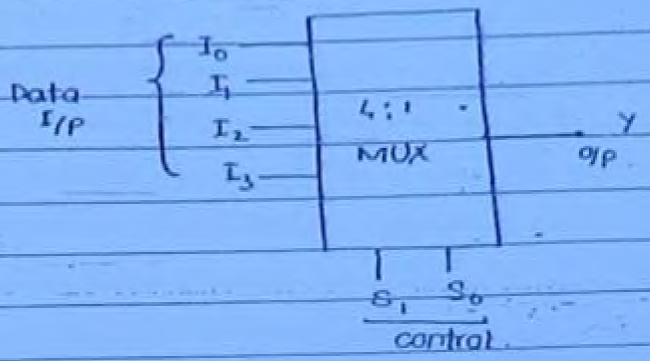
$= \bar{A}B + ABC$

$= B(\bar{A} + AC)$

$= B(\bar{A}+C)$

MULTIPLEXER

⇒ Many I/P and one O/P.



⇒ It is combinational circuits.

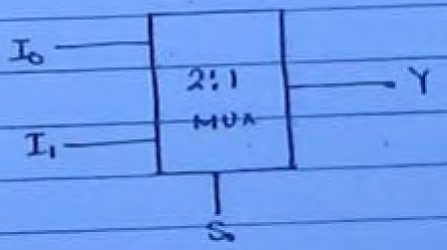
⇒ Depending on control or select I/P, one of the I/P is transfere to the O/P line.

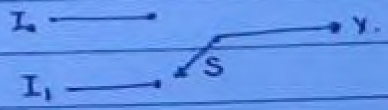
⇒ It is select I/P then also called as Data selector, or. Many to one ckt or, universal logic ckt or, parallel to serial s ckt.

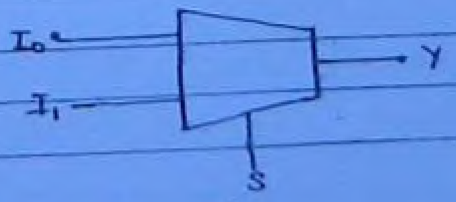
$$\boxed{\begin{aligned} m &= 2^n \\ \text{or, } n &= \log_2 m \end{aligned}}$$

where m = no. of data I/P.
n = no. of select i/P. (control I/P).

2:1. MUX :-







(symbol of MUX)

classmate

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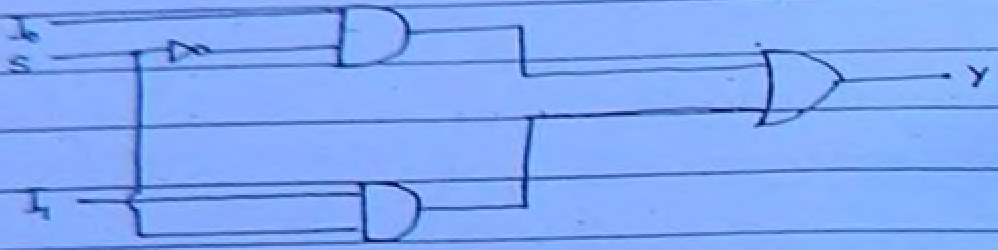
(ii) Truth table :-

S	Y
0	I_0
1	I_1

(iii) logical expression :-

$$Y = \bar{S} I_0 + S I_1$$

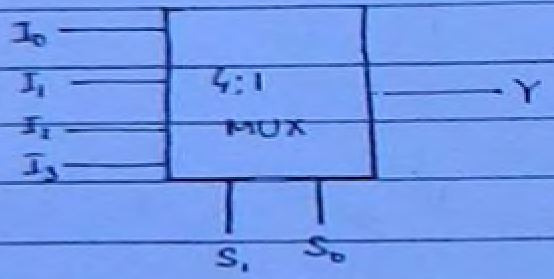
(iv) Implementation :-



⇒ In MUX, generally AND gate followed by OR gate.

4:1 MUX :-

(i)

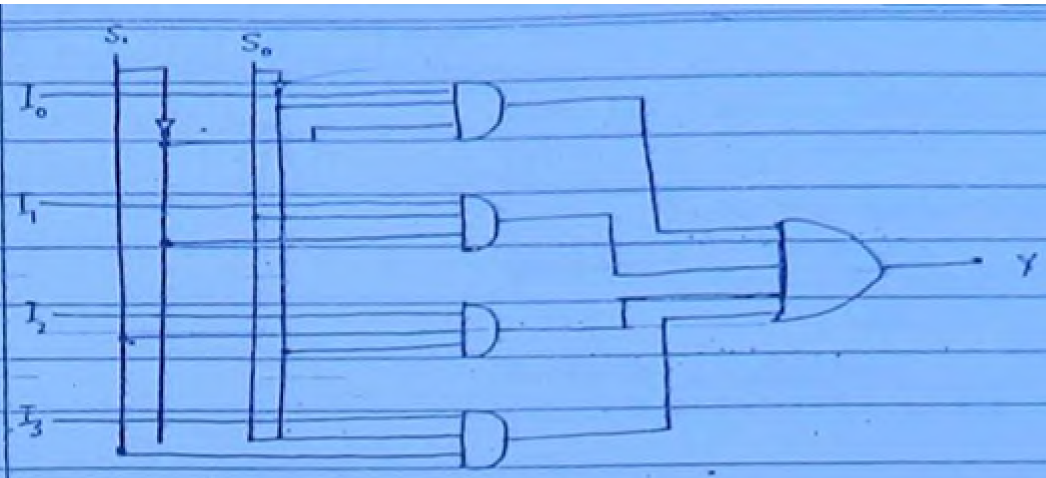


(ii) Truth table :-

S_1	S_0	Y
0	0	I_0
0	1	I_1
1	0	I_2
1	1	I_3

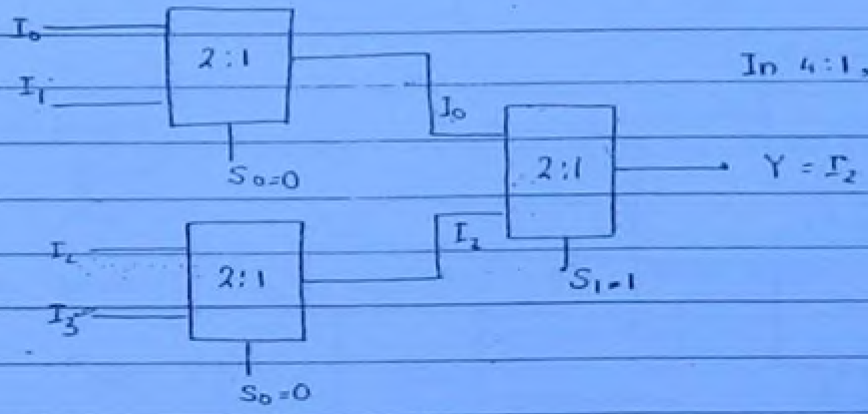
(iii) logical expression :-

$$Y = \bar{S_1}\bar{S_0} I_0 + S_0 \bar{S_1} I_1 + S_1 \bar{S_0} I_2 + S_1 S_0 I_3$$



I. Implementation of higher order MUX with lower order:-

(A) Implement 4:1 MUX using 2:1 mux:-



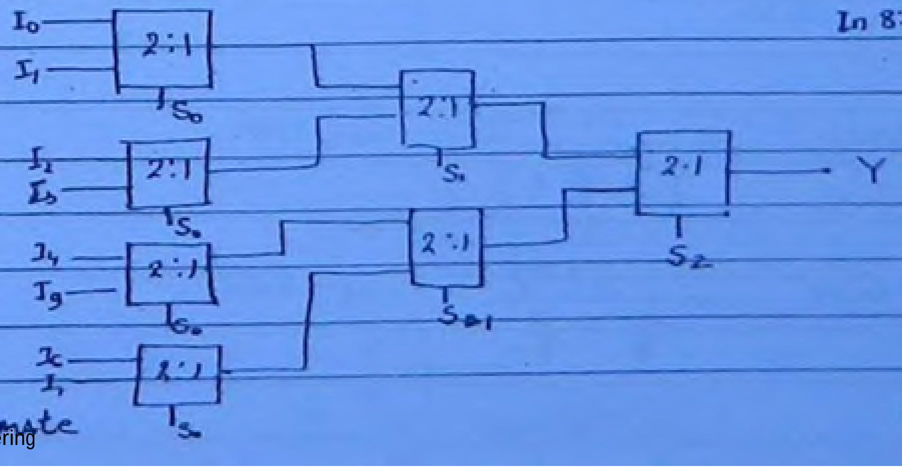
In 4:1, no. of 2:1 MUX = 3

$S_1 S_0$	—	Y
1 0		I_2

(B) Implement 8:1 MUX using 2:1 MUX:-

$$\text{no. of MUX} = \frac{8}{2} + \frac{4}{2} + \frac{2}{2} = 4+2+1 = 7$$

In 8:1, no. of 2:1 MUX = 7



(C) 16×1 $\xrightarrow[\text{15 MUX}]{8+4+2+1}$ 2×1 MUX

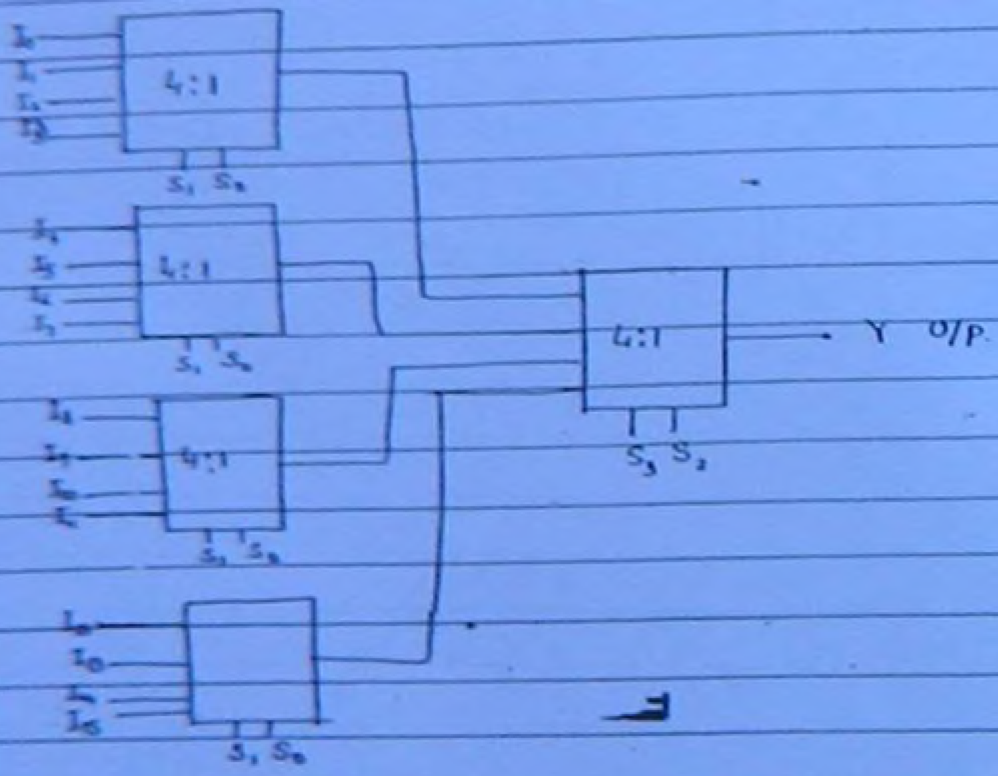
(D) 64×1 $\xrightarrow[32+16+8+4+2+1]{\text{63 MUX}}$ 2×1 MUX

(E) 256×1 $\xrightarrow[128+64+32+16+8+4+2+1]{\text{255 MUX.}}$ 2×1 MUX

⇒ Therefore for $2^n \times 1$ MUX the no. of 2:1 mux is $2^n - 1$. MUX required.

(F) 16×1 MUX from 4×1 MUX :-

no. of MUX = $\frac{16}{4} + \frac{4}{4} = 4+1 = 5$.



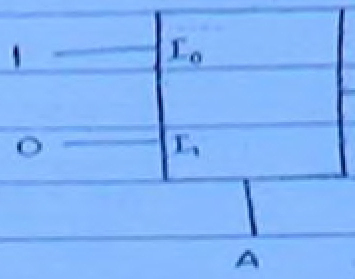
(G) 16×1 MUX $\xrightarrow[\frac{64}{4}+\frac{16}{4}+\frac{4}{1}]{\text{21 MUX}}$ 4:1 MUX

(H) 64×1 MUX $\xleftrightarrow[\frac{64}{8}+\frac{8}{8}]{\text{9 MUX}}$ 8:1 MUX

II MUX as universal :-

☆ 2:1 MUX :-

NOT :-

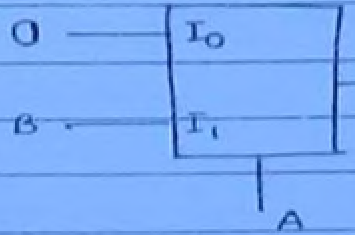


$$Y = \bar{S_0} I_0 + S_0 I_1$$
$$= \bar{A} \times 1 + 0 \times A$$
$$= \bar{A}$$

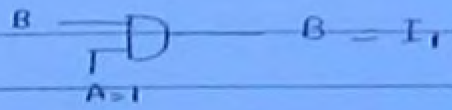
A	Y
0	1
1	0

⇒ 1 - MUX is required for NOT Gate.

AND :-

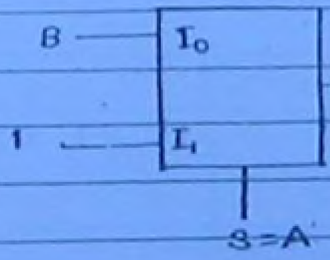


$$Y = \bar{A} \times 0 + AB$$
$$= AB$$



⇒ 1 - MUX (2:1) is required for AND Gate.

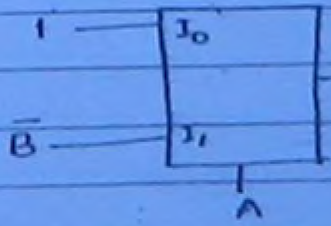
OR :-



$$Y = \bar{A}B + A \times 1$$
$$= A + B.$$

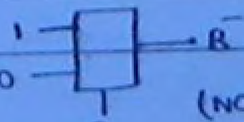
⇒ 1 MUX (2:1) is required for OR gate.

NAND :-



$$Y = \bar{A} \times 1 + \bar{B}A$$
$$= \bar{A} + \bar{B}$$
$$= \overline{AB}$$

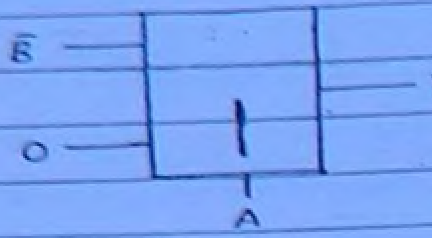
for $\bar{B}$:-



(NOT gate).

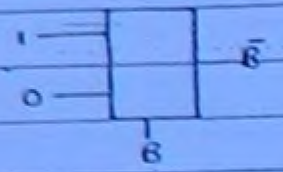
⇒ 2-MUX required for NAND gate.

NOR :-



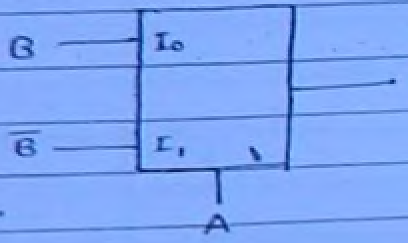
$Y = \bar{A}\bar{B} + A*0$
$= \overline{A+B}$

for $\bar{B}$ ⇒



⇒ 2 MUX (2:1) required for NOR gate.

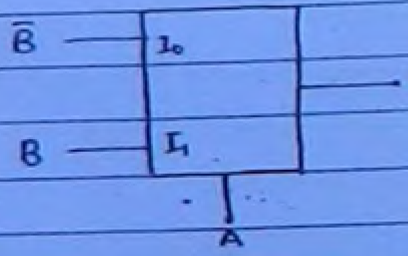
EXOR :-



$Y = B\bar{A} + \bar{B}A$

⇒ 2 MUX (2:1) required for EXOR gate.

EXNOR :-



$Y = \bar{A}\bar{B} + AB$

⇒ 2 MUX (2:1) required for EXNOR gate.

Ques:- EXOR , AND gate required 2x1 MUX.

(a) 1,1
✓(b) 2,1
(c) 1, 2
(d) 2.2

Sol:- EXOR = 2 , AND = 1

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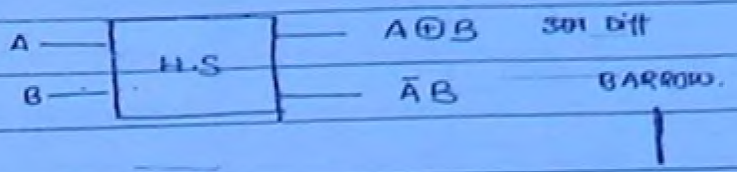
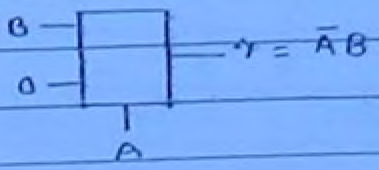
⇒ for HA – 3 Mux required (2:1)

⇒ for HS – 3 Mux required (2:1)



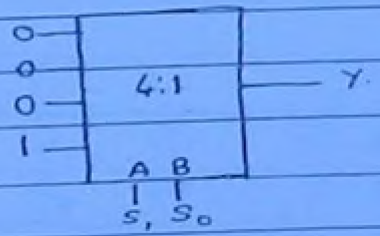
A⊕B = 2 MUX required and.

ĀB = 1 MUX.

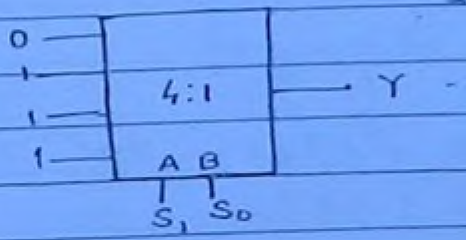


☆ 4:1 MUX :-

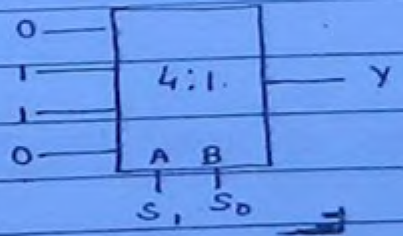
AND :-



OR :-

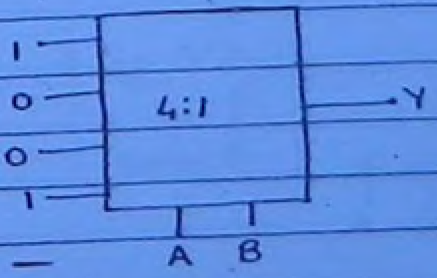


EXOR :-



⇒ Any two variable function is implemented with 4:1 MUX.

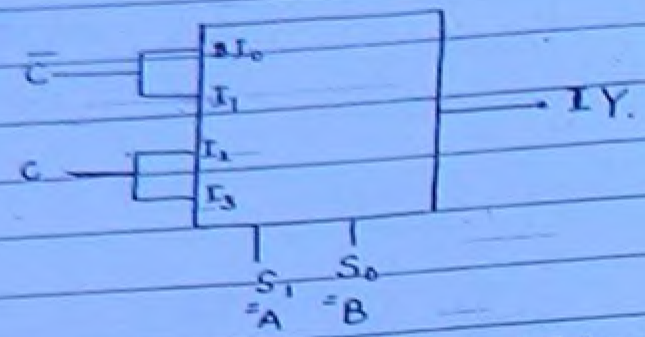
EXNOR :-



III Determine minimize o/p logical expression:-

Simplify:-

Q:-



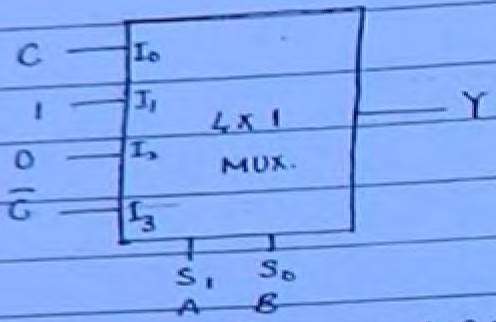
Sol:- $Y = \bar{A}\bar{B}\bar{C} + \bar{A}B\bar{C} + A\bar{B}C + ABC$

$= \bar{A}\bar{C}(B+\bar{B}) + AC(\bar{B}+B)$

$= \bar{A}\bar{C} + AC$

$= A \odot C$

Q:-



Sol:- $Y = \bar{A}\bar{B}C + \bar{A}B + A\bar{B}\times 0 + AB\bar{C}$

$= \bar{A}\bar{B}C + \bar{A}B + AB\bar{C}$

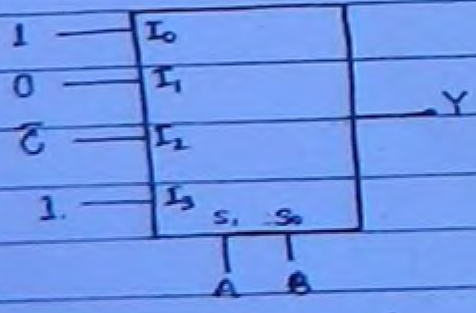
$= \bar{A}C + B\bar{C}$

A \ BC	$\bar{B}\bar{C}$	$\bar{B}C$	BC	$B\bar{C}$
$\bar{A}$		1	1	1
A				1

IV. Implementation of given logical expression:-

Q:- $f(A,B,C) = \Sigma m(0,1,4,6,7)$

Sol:-



	I_0	I_1	I_2	I_3
$\bar{C}$	⓪	2	④	⑥
C	①	3	5	⑦
	1.	0	$\bar{C}$	1.

A	B	C			
0	0	0 → $\bar{C}$		$\bar{B}$	$\bar{A}$
0	0	1 → C		$\bar{B}$	$\bar{A}$
0	1	0 → $\bar{C}$		B	$\bar{A}$
0	1	1 → C		B	$\bar{A}$
1	0	0 → $\bar{C}$		$\bar{B}$	A
1	0	1 → C		$\bar{B}$	A
1	1	0 → $\bar{C}$		B	A
1	1	1 → C		B	A

⇒ 1 - 4:1 MUX and 1 - NOT Gate required.

Q:- Implement logical expression.

$f(A,B,C) = (1,2,3,5,6,7) m\Sigma$

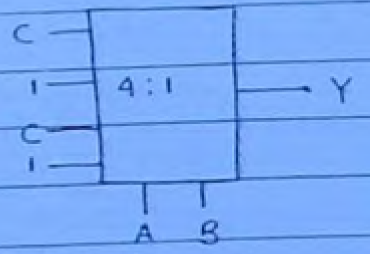
(i) AB as select line

(ii) AC

(iii) BC

Sol:- (i)

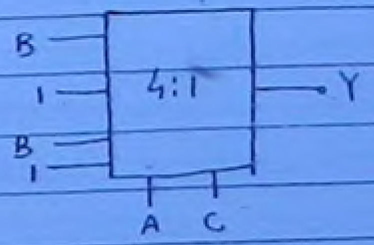
	I_0	I_1	I_2	I_3
$\bar{C}$	0	②	4	⑥
C	①	③	⑤	⑦
\	C	1	C	1



⇒ 1 - 4:1 MUX required.

(ii)

	$\bar{A}\bar{C}$ I_0	$\bar{A}C$ I_1	AC I_2	AC I_3
$\bar{B}$	0	①	4	⑤
B	②	③	⑥	⑦
	B	1	B	1



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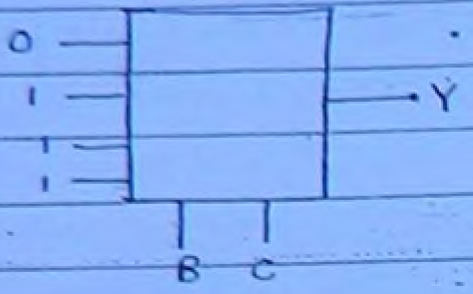
(iii) BC control :-

	I_0	I_1	I_2	I_3
$\bar{A}$	0	①	②	③
A	4	⑤	⑥	⑦
	0	1	1	1



⇒ using one 4:1 MUX → Any two variable function implement
→ some of three variable implement.

⇒ one 4x1 MUX and one NOT → All Two → implement
→ All Three → implement

⇒ one 8x1 MUX → all Three
→ Some four.

⇒ one 8x1 MUX and one NOT → All Three are ~~four~~ implement
→ All Four are implemented

JTO-2009

Ques :- $f = \pi M(0,1,4,7)$

Sol :- first convert it into minterm expression $f = \Sigma m(2,3,5,6)$

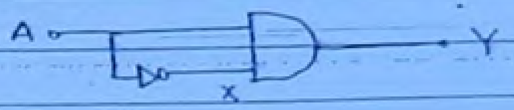
Hazard :-

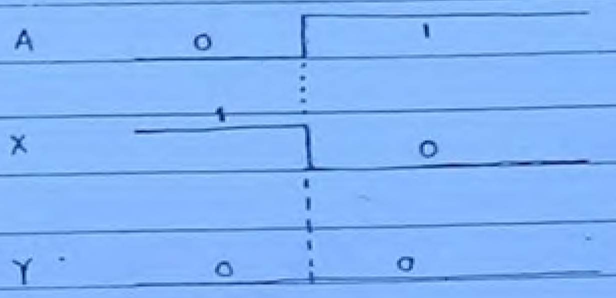
⇒ Hazard is occurs due to propogation delay of the logic ckt.

⇒ This is unwanted change at the o/p.

Q) For the give ckt Determine o/p waveform when no propagati

delay.



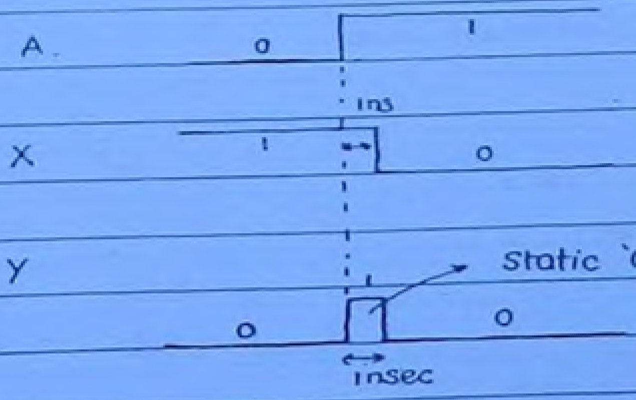


static '0'.

case II :-

If there is propagation delay of 1ns in NOT gate an

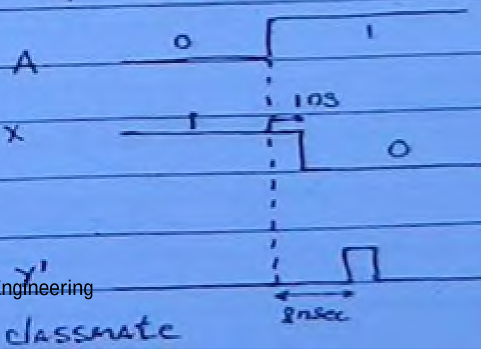
no delay in AND gate.



Static '0' Hazard.

case III :-

If t_{pd} (NOT) = 1nsec , t_{pd} (AND) = 2nsec.



classmate

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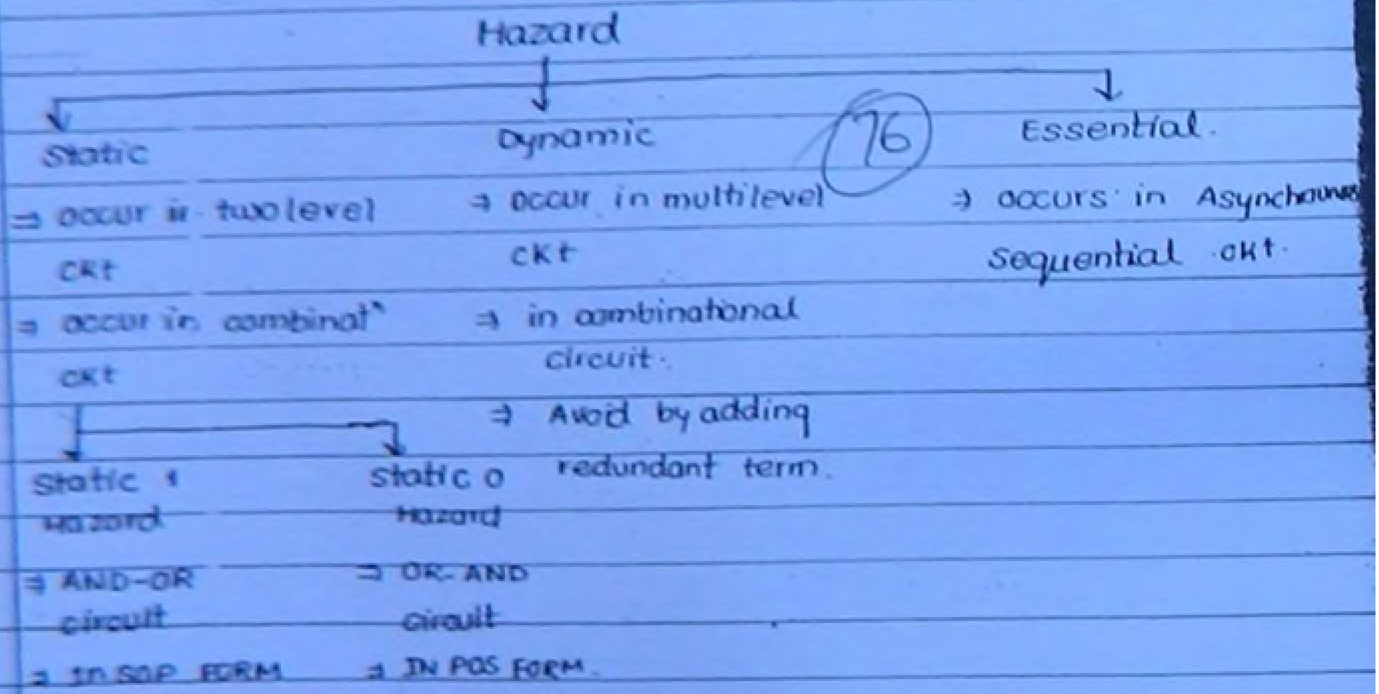


Static:
⇒ occur in two level ckt
⇒ occur in combinatn ckt

Dynamic:
⇒ occur in multilevel ckt
⇒ in combinational circuit.
⇒ Avoid by adding redundant term.

Essential:
⇒ occurs in Asynchoun sequential ckt.

Static 1 Hazard:
⇒ AND-OR circuit
⇒ In SOP FORM

Static 0 Hazard:
⇒ OR-AND circuit
⇒ IN POS FORM.

⇒ To avoid static and Dynamic Hazard redundant terms are added in combinational ckt.

⇒ Essential Hazard :- These Hazards can not be avoided but feels essential.

Memories

Primary → RAM, ROM

Secondary → Semi random, Serial access memory

RAM	ROM	Semi random	Serial access memory
⇒ Read/write	⇒ Read only	⇒ AI disk	⇒ magnetic tap
⇒ Random access	⇒ Random access	⇒ CD	⇒ Magnetic bubb
⇒ Voltaile	⇒ Non volataile	⇒ DVD	⇒ Ferrite core
⇒ Temparary data	⇒ Permanent data	⇒ HD	⇒ CCD (charged coupl device)
	BIOS/System program		

⇒ Ferrite core → DRO → Discrictive read only out.

RAM (Random access memory) :-

⇒ Each memory location if m bits are stored then memory capacity $(2^n \times m)$

⇒ with n-bit address - max. no. of memory location requir is $= 2^n$.

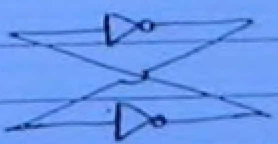
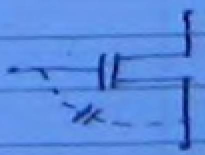
⇒ $4^K \times 8$ memory.

$= 2^2 \times 2^{10} \times 8 = 2^{12} \times 8$

= 12 - address line

8 - data lines.

RAM → Static, Dynamic

Static	Dynamic
1. Stored like FF	1. Data stored in MOS capac
	

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Memories

Primary → RAM, ROM

secondary → Semi random, Serial access memory

RAM	ROM	Semi random	Serial access memory
⇒ Read/write	⇒ Read only	⇒ All disk	⇒ magnetic tape
⇒ Random access	⇒ Random access	⇒ CD	⇒ Magnetic bubb
⇒ Voltaile	⇒ Non volataile	⇒ DVD	⇒ Ferrite core
⇒ Temporary data	⇒ Permanent data	⇒ HD	⇒ CCD (charged coupl device)
	BIOS/System program		

⇒ Ferrite core → DRO → Discrictive read only out.

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$= 2^2 \times 2^{10} \times 8 = 2^{12} \times 8$

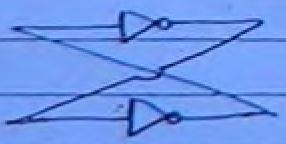
= 12 - address line

8 - data lines.

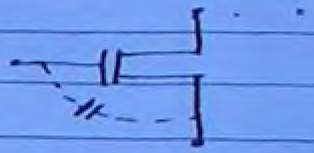
RAM

static | Dynamic

1. Stored like FF



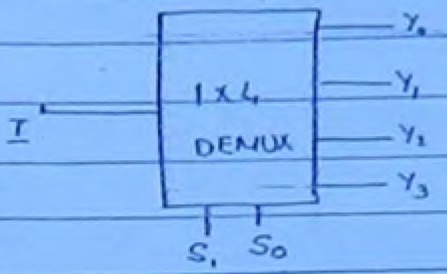
1. Data stored in MOS capac

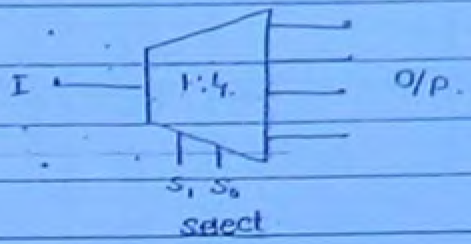


79

DEMUX (DEMULTIPLEXER) :-

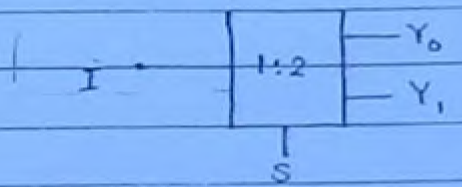
⇒ Single I/P and Many O/P.





⇒ DEMUX is combinational ckt which have one I/P and may O/P deper
on select I/P., I/P is transfered to any of the O/P.

⇒ Also known as 1 to many ckt or, data distributor.



Truth table :-

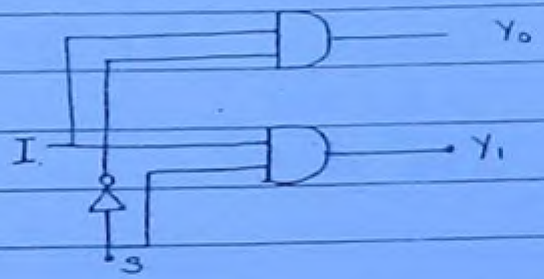
S	Y_1	Y_0
0	0	I
1	I	0

Expression :-

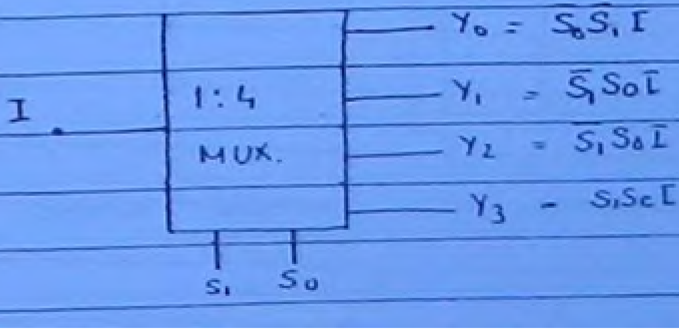
$Y_0 = \bar{S} I$

$Y_1 = S I$

implementation :-



~~4x or~~ 1:4 DEMUX :-

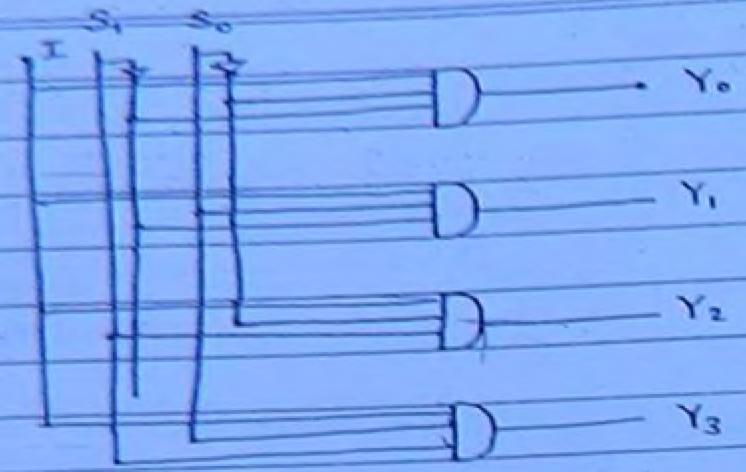


$Y_0 = \bar{S_0}\bar{S_1} I$

$Y_1 = \bar{S_1} S_0 I$

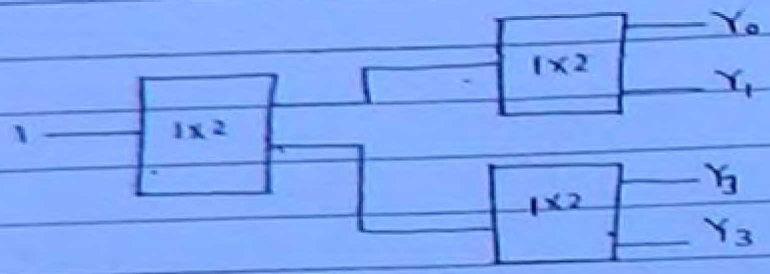
$Y_2 = \bar{S_1} S_0 I$

$Y_3 - S_1 S_0 I$



Implementation of Higher oder DEMUX from lower order:

(i) 1X4 DEMUX $\xleftrightarrow{3}$ 1X2 DEMUX



(ii) 1X8 DEMUX $\xleftrightarrow{7}$ 1X2 DEMUX

(iii) 1X16 DEMUX $\xleftrightarrow{5}$ 1X4 DEMUX

(iv) 1X64 DEMUX $\xleftrightarrow{21}$ 1X4 DEMUX $\quad \frac{64}{4} + \overbrace{\frac{16}{4} + \frac{4}{4} + 1}^{21}$

(v) 1X64 DEMUX $\xleftrightarrow{9}$ 1X8 DEMUX

(vi) 1X256 DEMUX $\xleftrightarrow{7}$ 1X16 DEMUX

DECODER :-

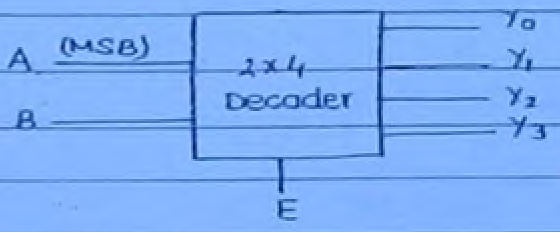
⇒ Decoder is a combinational ckt which have many I/P and m
O/P.

⇒ It is used to convert binary data to other code (binary to

eg. Binary to octal (3×8)
BCD to Decimal (4×10)
Binary to Hexadecimal
BCD to seven segment

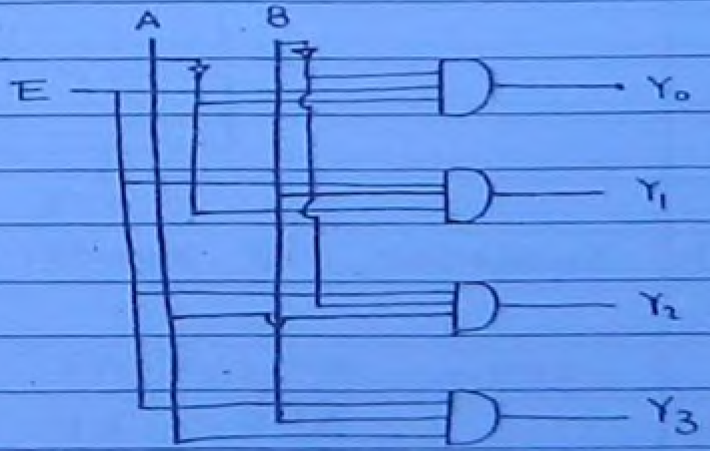
⇒ 2 to 4 decoder is minimum possible decoder.

2×4 Decoder :-



Truth table :-

E A B	Y_3	Y_2	Y_1	Y_0
0 x x	0	0	0	0
1 0 0	0	0	0	①
1 0 1	0	0	①	0
1 1 0	0	①	0	0
1 1 1	①	0	0	0



logical Expression :-

$Y_0 = \bar{A}\bar{B}E$
$Y_1 = \bar{A}BE$
$Y_2 = A\bar{B}E$
$Y_3 = ABE$

⇒ Decoder and DEMUX internal ckt remains sam.

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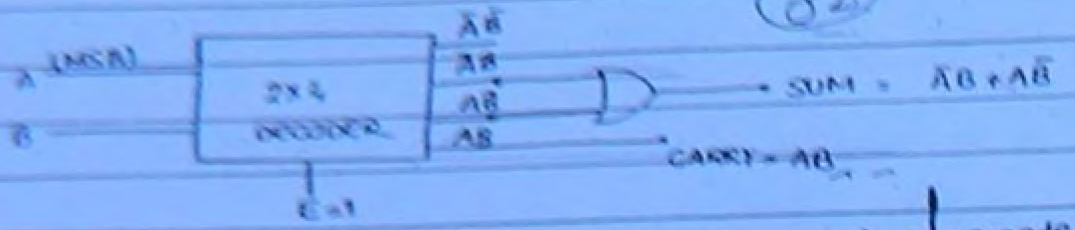
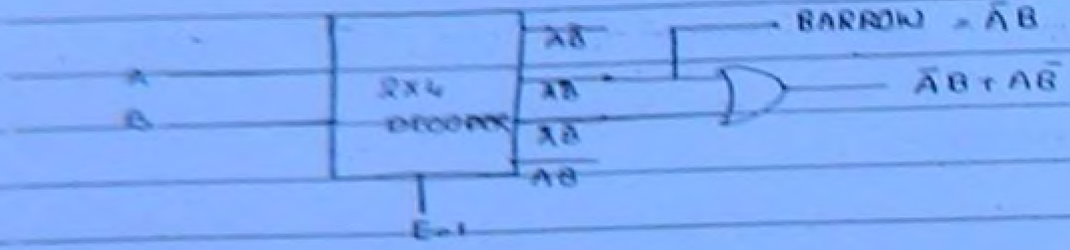
Q:- Implement Half adder using 2x4 Decoder.

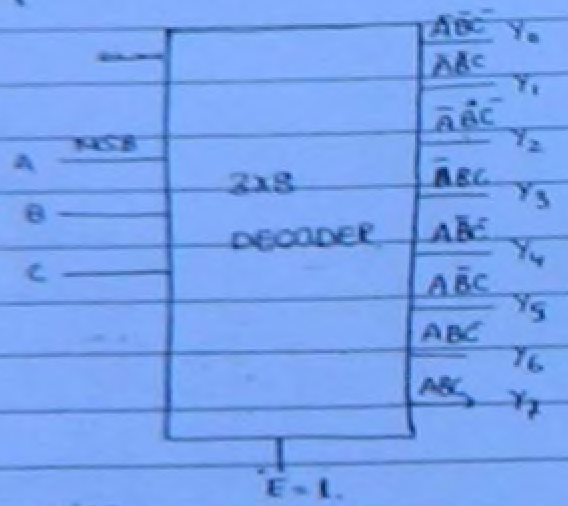


⇒ We implement HA using 1 - 2x4 Decoder and 1 OR gate and same for HS.



Binary to octal DECODER :-

⇒ Also called as 3x8 decoder.



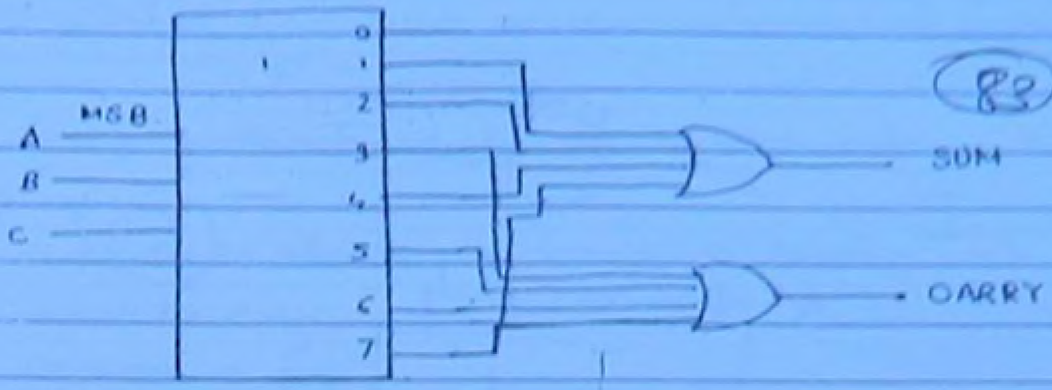
Q:- Implement using 3x8 Decoder make FA.

Sol:-

SUM = $\Sigma m(1,2,4,7)$

$= \bar{A}\bar{B}C + \bar{A}B\bar{C} + A\bar{B}\bar{C} + ABC$

CARRY = $\Sigma m(3,5,6 7)$

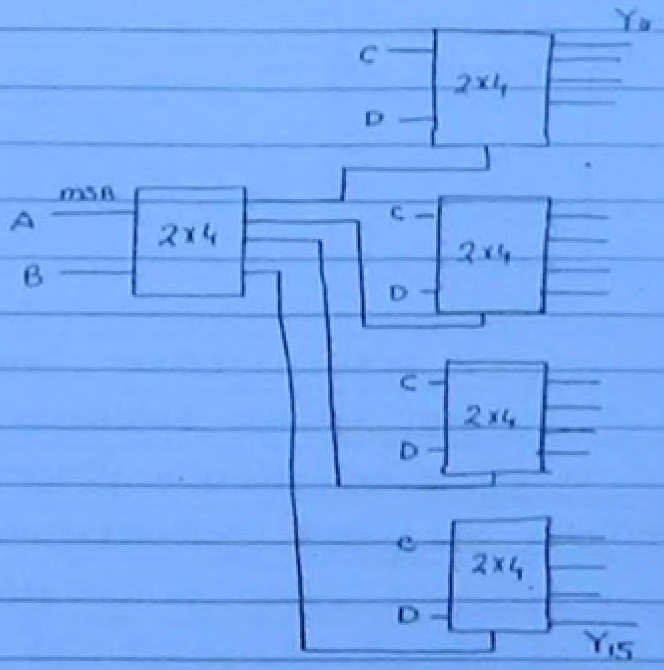


Q:- Implementation of Higher order decoder using lower order:-

4 x 16 $\xleftrightarrow{5}$ 2x4 → (Since 2x4 Decoder means 1x4 DEMUX using 2 select line

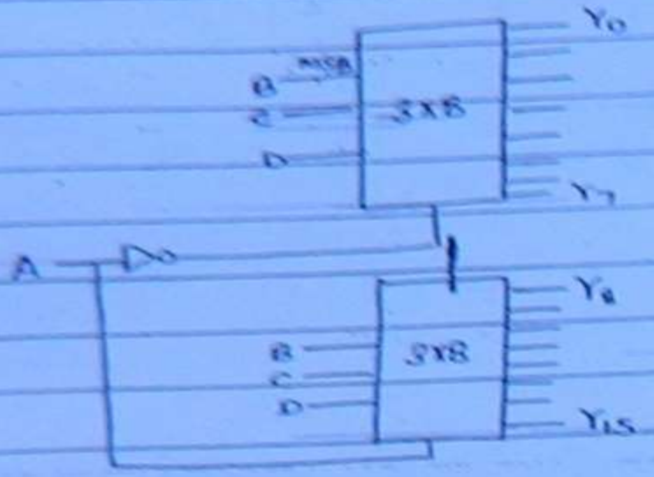
{ 1x16 $\xleftrightarrow{5}$ 1x4]

{ 16x1 $\xleftrightarrow{5}$ 4x1 }



⇒ ~~4 16~~ 6 x 64 $\xleftrightarrow{21}$ 2x4

⇒ 8 x 256 $\xleftrightarrow{17}$ 4x16


Y0
B
MSB
C
D
3x8
Y7
A
Y8
B
C
D
3x8
Y15

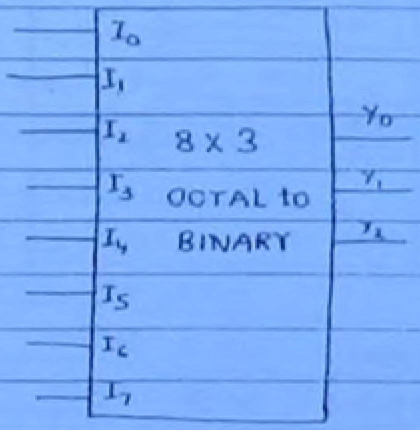
ENCODER :-

⇒ Encoder is the combinational ckt which have many I/P and many O/P.

⇒ Encoder is used to convert other code to Binary.

- octal to Binary
- Decimal to BCD
- Hexadecimal to Binary.

Octal to Binary Encoder :-



⇒ In normal encoder one of the I/P line is high and correspon Binary available at the O/P.

⇒ In priority encoder no. of I/P is high. only highest priority no. corresponding Binary is available at the O/P.

Truth table :-

I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	0	0	0	1
0	0	0	0	0	1	0	0	0	1	0
0	0	0	0	1	0	0	0	0	1	1
0	0	0	1	0	0	0	0	1	0	0
0	0	1	0	0	0	0	0	1	0	1
0	1	0	0	0	0	0	0	1	1	0
1	0	0	0	0	0	0	0	1	1	1

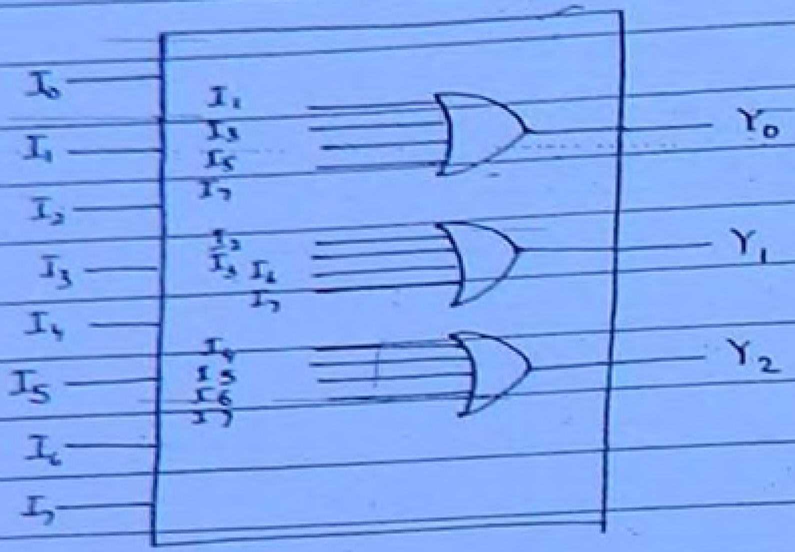
logical expression:-

$Y_0 = I_1 + I_3 + I_5 + I_7$

$Y_1 = I_2 + I_3 + I_6 + I_7$

$Y_2 = I_4 + I_5 + I_6 + I_7$

86



⇒ Decoder contains AND Gate.

⇒ DEMUX contains AND Gate

⇒ ENCODER contains OR Gate.

FLIP-FLOP

DATE

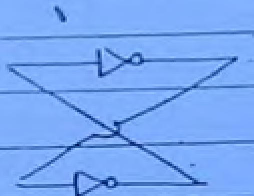
- ⇒ It is basic memory element.
- ⇒ It can store 1 bit.
- ⇒ FF have two o/p which have complemented to each other
- ⇒ It have two stable state hence it is known as bistable multivibrator.

CONTENT :-

0. SR latch → NAND
   → NOR

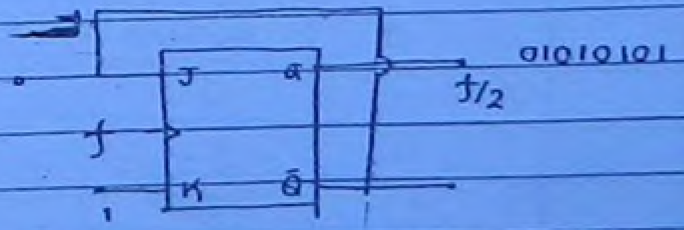
1. SR FF
2. JK FF
3. D FF
4. T FF

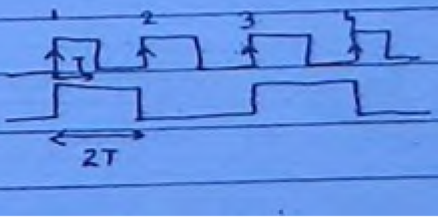
- ⇒ CKts
- ⇒ Truth table
- ⇒ characteristic table
- ⇒ characteristic equation.
- ⇒ Excitation table.
- ⇒ conversion from one to another
- ⇒ simple CKt.


latch

⇒ using Not gate the problem is, it have only one I/P then we use NAND or NOR gate instead of NOT gate.

⇒ FF is not only used for storing 1 bit but it also used for frequency divider.





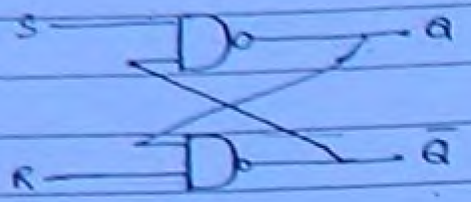
SR latch using NAND :-

NAND :-

enable - 1.

Disable - 0

A B	Y
0 0	1
0 1	1
1 0	1
1 1	0

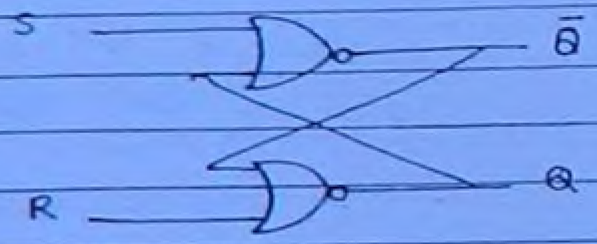


Truth table :-

S	R	Q
0	0	Invailid $(Q = \bar{Q} = 1)$
0	1	1
1	0	0
1	1	Previous state (no change)

⇒ In SR latch if both gates are enabled o/p remains same previous state and both are disable then o/p remains same invailid state.

SR latch using NOR gate :-



∵ NAND enable is 1 and disable is 0

and, in NOR - E = 0

D = 1.

⇒ then we change Q and $\bar{Q}$ position

Truth table :-

S	R	Q
0	0	Previous state.
0	1	0
1	0	1
1	1	invalid $(Q = \bar{Q} = 0)$

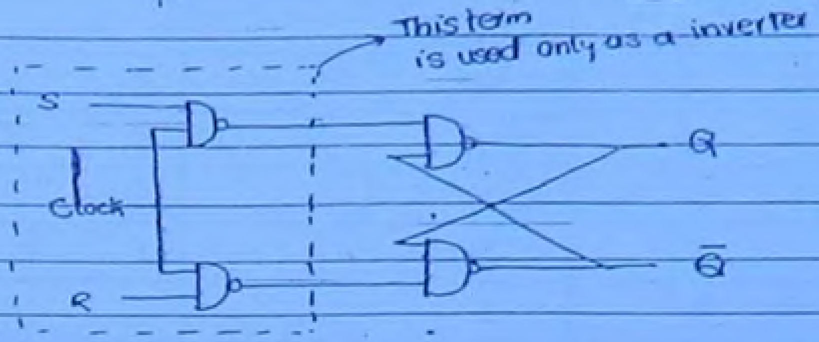
A B	Y
0 0	1
0 1	0
1 0	0
1 1	0

⇒ SR latch is used to eliminate switch bouncing.

⇒ Bouncing means vibration of switches when ON or OFF

SR Flip Flop :–

S = Set
R = Reset

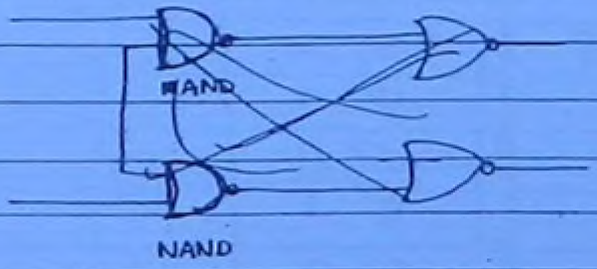


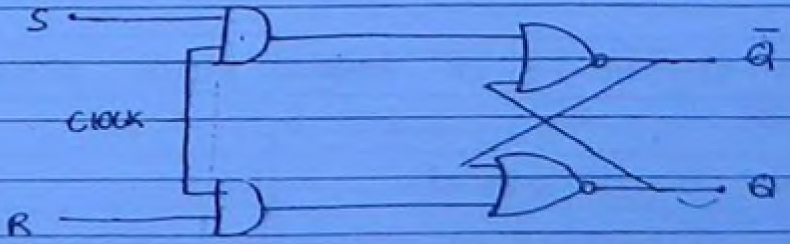
Truth table :-

Clock	S	R	Q_{n+1}	
0	*	*	Previous state (Q_n)	} → Hold state
1	0	0	Q_n	
1	0	1	0 → Reset	
1	1	0	1 → Set	
1	1	1	invailid. → unused	

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	invailid.

← very imp_





⇒ Truth table is same as for NAND gate SR FF.

Characteristic table :-

S	R	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	X
1	1	1	X

S	R	Q_{n+1}
0	0	Q_n
0	1	0
1	0	1
1	1	invailid

S \ RQ_n	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
$\bar{S}$		1		
S	1	1	x	x

$$Q_{n+1} = S + \bar{R}Q_n$$

$$\boxed{Q_{n+1} = S + \bar{R}Q_n} \text{ and } SR = 0 \text{ ——— (1)}$$

⇒ since S=1, R=1. the o/p is invailid because S·R=1 not satisfy the above condition.

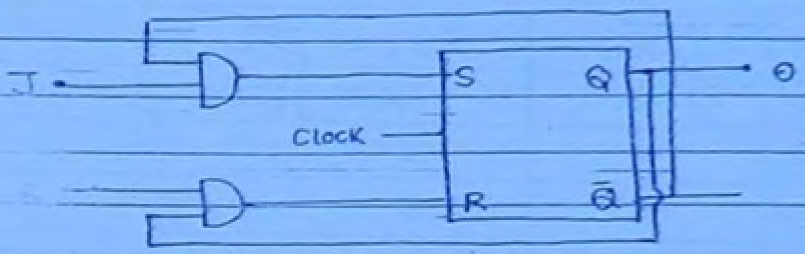
Excitation table :-

Q_n	Q_{n+1}	S	R
0	0	0	*
0	1	1	0
1	0	0	1
1	1	x	0

⇒ Disadvantage of SR FF is invailid state present when S=1 and R=1.

⇒ To avoid this JK FF is used.

JK Flip Flop :-



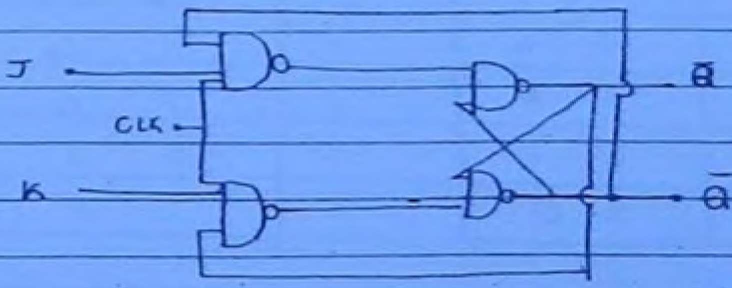
$S = J\bar{Q}$

$R = KQ$

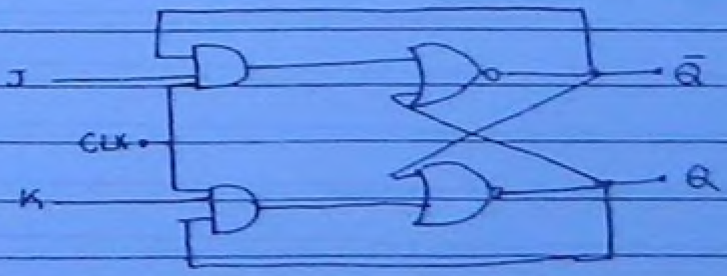
Clock	J	K	Q_{n+1}
0	x	x	Q_n
1	0	0	Q_n
1	0	1	0
1	1	0	1
1	1	1	$\bar{Q}_n$

J	K	Q_{n+1}	
0	0	Q_n	Hold
0	1	0	Reset
1	0	1	Set
1	1	$\bar{Q}_n$	Toggle.

J-K FF using NAND gate :-



J-K FF using NOR gate :-



JK FF characteristic table :-

J	K	Q_n	Q_{n+1}
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

logical Expression :-

minimization :-

J \ KQ_n	$\bar{K}\bar{Q}_n$	$\bar{K}Q_n$	KQ_n	$K\bar{Q}_n$
$\bar{J}$		1		
J	1	1		1

$$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$$

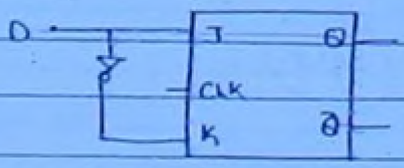
$$\boxed{Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n}$$

Exitation table :-

Q_n	Q_{n+1}	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

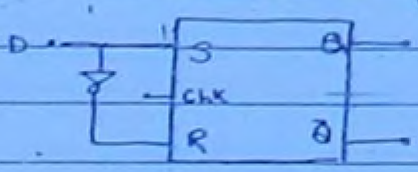
⇒ Drawback in JK ff is Race arround condition which is eliminated in D flipflop.

D-Flip Flop :-



J = D

K = $\bar{D}$



S = D

R = D

Truth table :-

CLK	D	Q_{n+1}
0	*	Q_n
1	0	0
1	1	1

D	Q_{n+1}
0	0
1	1

Characteristic table :-

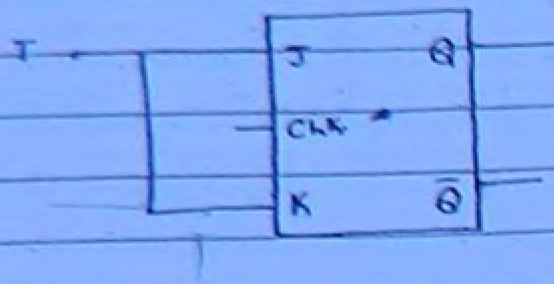
D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

$\boxed{Q_{n+1} = D}$ → Therefore it is also called transparent latc

Excitation table :-

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

T Flip-Flop (Toggle) :-



J = K = T

Truth table :-

Clk	~~J~~	~~K~~	T	Q_{n+1}
0	~~x~~	~~x~~	x	Q_n
1	~~0~~		0	Q_n
1			1	$\overline{Q}_n$

T	Q_{n+1}
0	Q_n
1	$\overline{Q}_n$

Characteristic table :-

T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

$$\boxed{Q_{n+1} = TQ_n + T\overline{Q}_n = T \oplus Q_n}$$

Excitation table :-

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

Important :-

	J	K	Q_{n+1}	
SR-FF	0	0	Q_n	T-FF
	0	1	0	D-FF
	1	0	1	
	1	1	Q_n	

⇒ ∵ All tables are inside JK FF therefore it is also called as JK FF universal flip flop.

Excitation table :-

Q_n	Q_{n+1}	S	R	J	K	D	T
0	0	0	X	0	X	0	0
0	1	1	0	1	X	1	1
1	0	0	1	X	1	0	1
1	1	X	0	X	0	1	0

FF → Flip Flop - one bit storing element

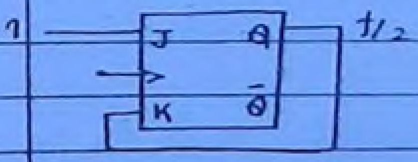
$Q_{n+1} = S + \bar{R}Q_n$ ⇒ SR = Set Reset

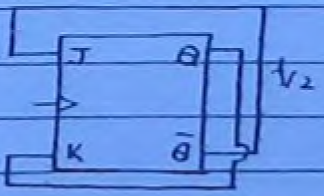
$Q_{n+1} = J\bar{Q}_n + \bar{K}Q_n$ ⇒ JK = name of person who give the IC

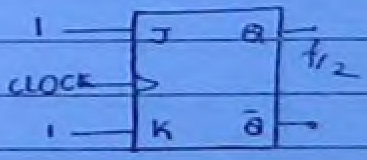
$Q_{n+1} = D$ ⇒ D = Delay element

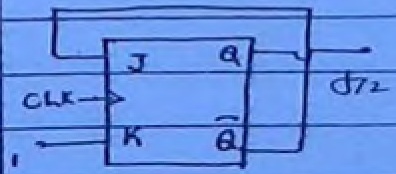
$Q_{n+1} = T \oplus Q_n$ ⇒ T = Toggle

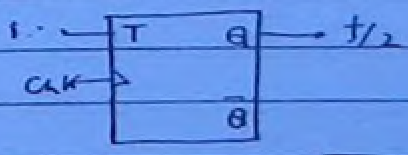
Toggle mode of JK :-

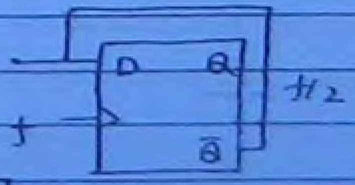




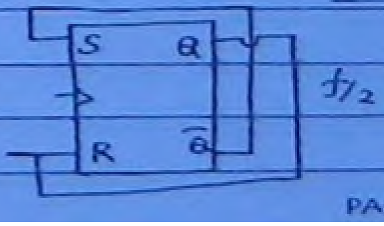


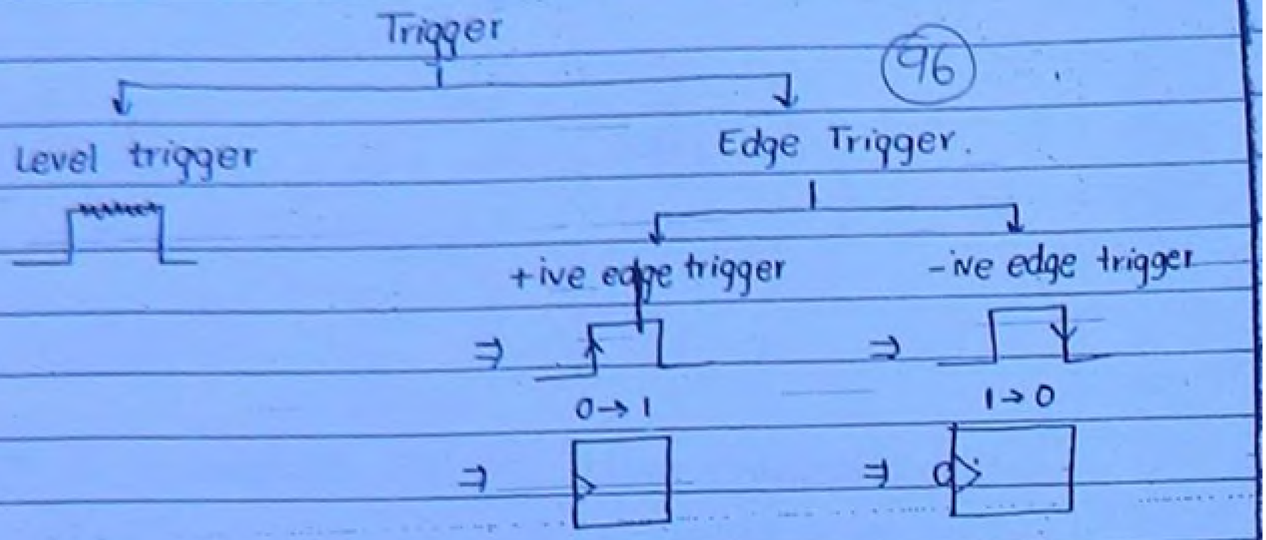






All 7 diagram is in Toggle mode

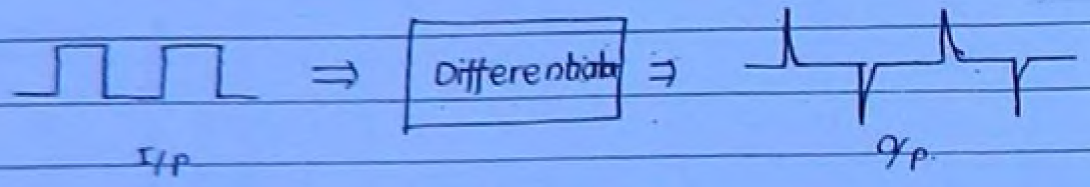




⇒ In level trigger ckt, o/p may changes many time in single clock

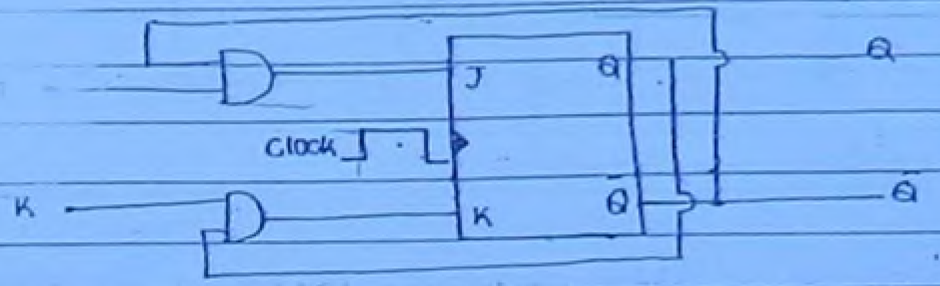
⇒ In edge trigger, o/p may change only ones in single pulse.

⇒



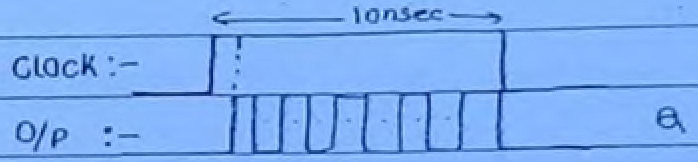
Race Arround condition :-

⇒ occurs in JK flip-flop (Draw back)



if t_{pw} = 10nsec

t_{pFF} = 1nse. Then :-



⇒ Then. To remove race arround condition :-

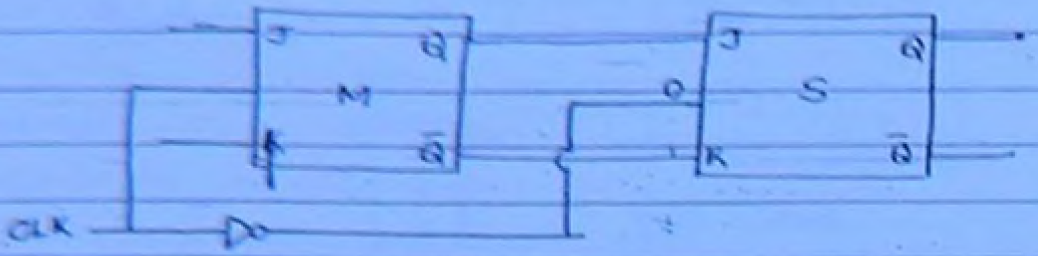
~~$t_{pdFF} << t_{pdclock}$~~ $\boxed{t_{pdclock} << t_{pdFF}}$

⇒ In JK FF. RAC occurs when J = K = 1. then ~~to~~ and t_{pdff} is less more than that of $t_{pdclock}$. and therefore the O/P is changes several time in single clock pulse.

Condition to remove Race arround condition :-

(i) $t_{pdclock} << t_{pdFF}$
(ii) Use of Master slave flipflop.
(iii) To increase the propogation delay of JK flip flop.

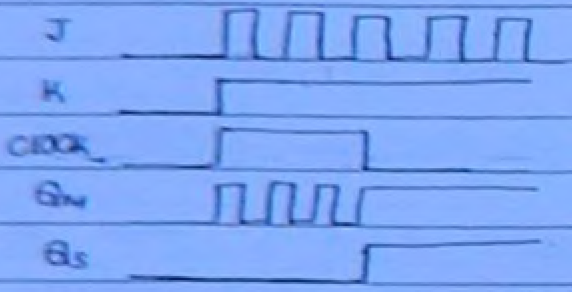
Master slave Flip Flop :-



⇒ Since the I/P of slave never go to (1,1) therefore in master slave the Race arround condition is removed.

⇒ Since I/P of slave is $J = Q$ and $K = \bar{Q}$ therefore it is always (1,0) or (0,1).

⇒ since race arround condition occurs only when the I/p is (1,1).



⇒ In M-S FF, O/P is change only when slave O/P is changing

⇒ In M-S FF, Master is ~~level~~ ~~triggered~~ and edge is slave is edge triggered.

⇒

Conversion of one ff to other FF :-

Procedure :-

⇒ Required FF characteristic table.

⇒ Available FF excitation table.

⇒ Write logical expression for excitation.

(i) JK-Flip Flop to D-Flip-Flop :-

D	Q_n	Q_{n+1}	J	K
0	0	0	0	x
0	1	0	x	1
1	0	1	1	x
1	1	1	x	0

⇒ write the logical expression for J and K :-

J =

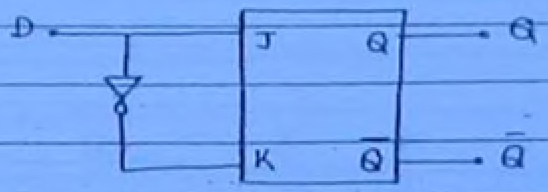
D \ Q_n		
$\bar{D}$		x
D	1	x

K =

D \ Q_n		
$\bar{D}$	x	1
D	x	

$J = D$ $\qquad$ $K = \bar{D}$

⇒ Implementation :-



Important :-

(A) SR to :-

(i) JK :- $S = J\bar{Q}$
$R = KQ$

(ii) D :- $S = D$
$R = \bar{D}$

(iii) T :- $S = T\bar{Q}$
$R = TQ$

(B) JK to :-

(i) SR :- $J = S$
$K = R$

(ii) D :- $J = D$
$K = \bar{D}$

(iii) T :- $J = T$
$K = T$

(C) D to :-

(i) SR : $D = S + \bar{R}Q$

(ii) JK : $D = J\bar{Q} + \underline{\bar{K}Q}$

(iii) T : $D = T \oplus Q$

(D) T to :-

(i) SR : $T = S\bar{Q} + RQ$

(ii) JK : $T = J\bar{Q} + KQ$

(iii) D : $T = D \oplus Q$.

(ii) JK FF to SR FF :-

(101)

S	R	Q_n	Q_{n+1}	J	K
0	0	0	0	0	X
0	0	1	1	X	0
0	1	0	0	0	X
0	1	1	0	X	1
1	0	0	1	1	X
1	0	1	1	X	0
1	1	0	X	X	X
1	1	1	X	X	X

0 0	0 X
0 1	1 X
1 0	X 1
1 1	X 0

J ⇒

S \ RQ_n				
$\bar{S}$		X	X	
S	1	X	X	X

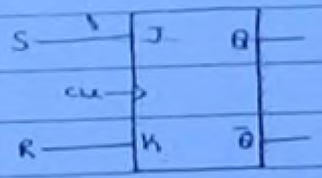
K ⇒

S \ RQ_n	$\bar{R}\bar{Q}_n$	$\bar{R}Q_n$	RQ_n	$R\bar{Q}_n$
	X		1	X
	X		X	X

$J = S$

$K = R$

implementation:-



(iii) JK FF to T FF :-

T	Q_n	Q_{n+1}	J	K
0	0	0	0	X
0	1	1	X	0
1	0	1	1	X
1	1	0	X	1

J :-

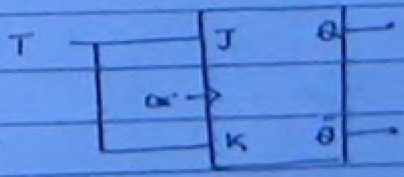
T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$		X
T	1	X

K :-

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	X	
T	X	1

$J = T$, $K = T$

implementation:-



classmate

Q_n	Q_{n+1}	S	R
0	0	0	x
0	1	1	0
1	0	0	1
1	1	x	0

(iv) SR to JK FF :-

J	K	Q_n	Q_{n+1}	S	R
0	0	0	0	0	x
0	0	1	1	x	0
0	1	0	0	0	x
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	1	x	0
1	1	0	1	1	0
1	1	~~0~~1	0	0	1

S :-

J \ $K\bar{Q}_n$, $\bar{K}\bar{Q}_n$				$K\bar{Q}_n$
$\bar{J}$		x		
J	1	x		1

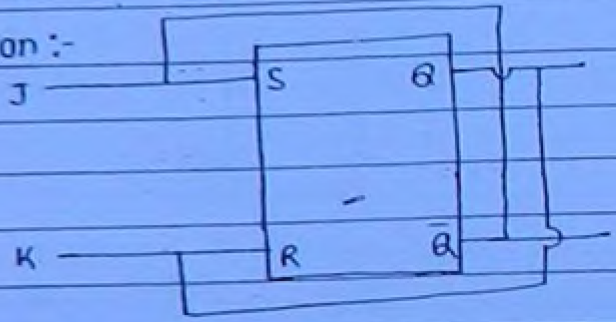
R :-

J \ KQ_n			KQ_n	
J	x		1	x
$\bar{J}$			1	

$S = J\bar{Q}_n$

$R = KQ_n$

Implementation :-



(v) SR FF to D FF :-

D	Q_n	Q_{n+1}	S	R
0	0	0	0	x
0	1	0	0	1
1	0	1	1	0
1	1	1	x	0

S :-

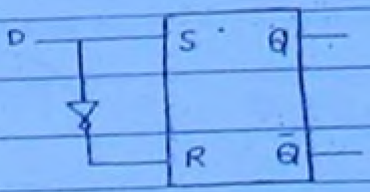
D \ Q_n		
$\bar{D}$		
D	1	x

R :-

D \ Q_n		
$\bar{D}$	x	1
D		

$R = \bar{D}$

implementation :-



(vi) SR to TFF :-

T	Q_n	Q_{n+1}	S	R
0	0	0	0	X
0	1	1	X	0
1	0	1	1	0
1	1	0	0	1

S :-

T \ Q_n	$\bar{Q}_n$	$\bar{Q}$
$\bar{T}$		X
T	1	

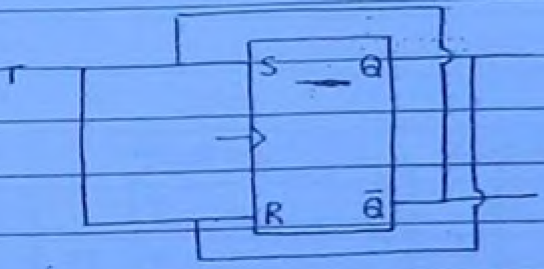
R :-

T \ Q_n	$\bar{Q}_n$	Q_n
$\bar{T}$	X	
T		1

$S = T\bar{Q}_n$

$R = TQ_n$

Implementation :-



(vii) D FF to SR FF :-

S	R	Q_n	$\bar{Q}_{n+1}$	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	X	X
1	1	~~0~~1	X	X

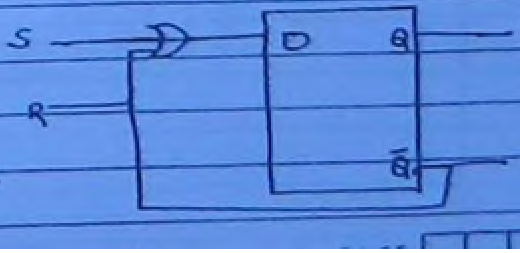
Q_n	Q_{n+1}	0
0	0	0
0	1	1
1	0	0
1	1	1

D :

S \ RQ_n				
$\bar{S}$		1		
S	1	1	X	X

1

$D = S + \bar{R}Q_n$



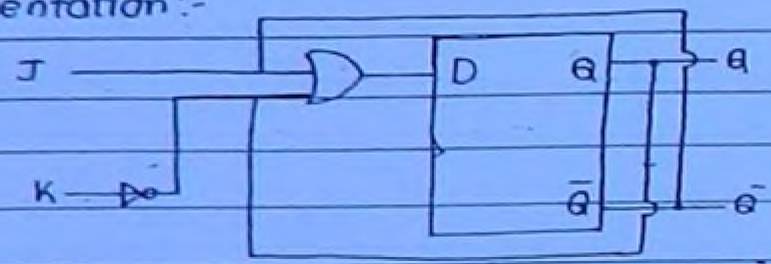
(viii) D FF to JKFF :-

J	K	Q_n	Q_{n+1}	D
0	0	0	0	0
0	0	1	1	1
0	1	0	0	0
0	1	1	0	0
1	0	0	1	1
1	0	1	1	1
1	1	0	1	1
1	1	1	0	0

J \ KQ_n	$\bar{K}\bar{Q}$	$\bar{K}\bar{Q}$	KQ	$K\bar{Q}$
D → $\bar{J}$		1		
J	1	1	0	1

$D = J\bar{Q} + \bar{K}Q$.

Implementation :-



(ix) D-FF to T FF :-

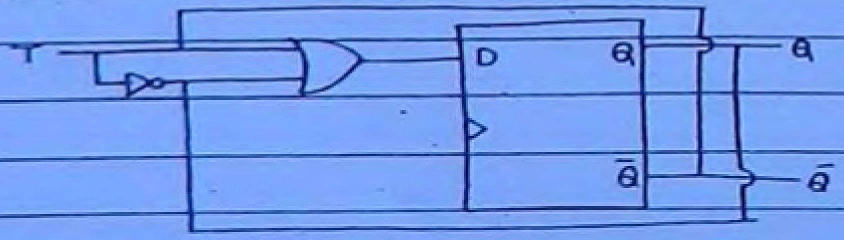
T	Q_n	Q_{n+1}	D
0	0	0	0
0	1	1	1
1	0	1	1
1	1	0	0

D =

Q_nF \ Q_n	$\bar{Q}$	Q
$\bar{T}$		1
T	1	

$D = \bar{T}Q + T\bar{Q}$

Implementation :-



(X) T FF to SR FF :-

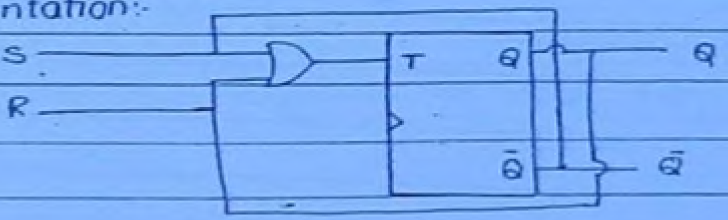
S	R	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	x	x
1	1	1	x	x

T :-

S \ RQ	$\bar{R}\bar{Q}$	$\bar{R}Q$	RQ	$R\bar{Q}$
$\bar{S}$			1	
S	1		x	x

$T = RQ + S\bar{Q}$

Implementation:-



(XI) T FF to JK FF :-

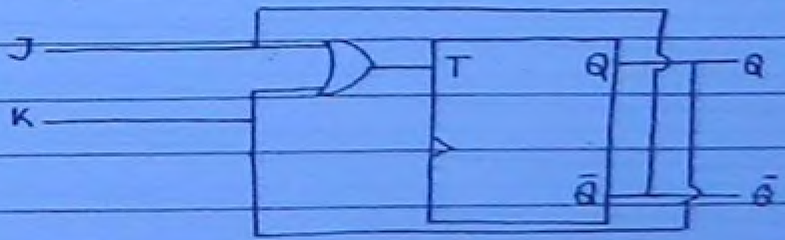
J	K	Q_n	Q_{n+1}	T
0	0	0	0	0
0	0	1	1	0
0	1	0	0	0
0	1	1	0	1
1	0	0	1	1
1	0	1	1	0
1	1	0	1	1
1	1	1	0	1

T :-

J \ KQ_n	$\bar{K}\bar{Q}$	$\bar{K}Q$	KQ	$K\bar{Q}$
$\bar{J}$			1	
J	1		1	1

$T = J\bar{Q} + KQ$

Implementation :-



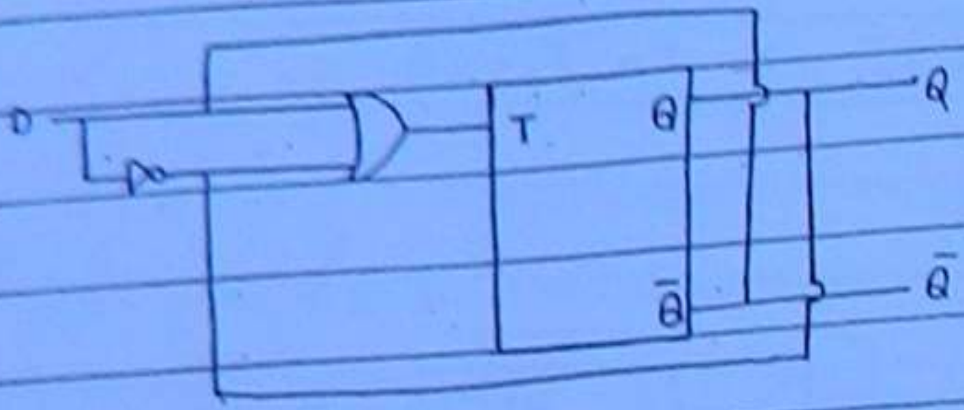
(xii) T-FF to D-FF :-

D	Q_n	Q_{n+1}	T
0	0	0	0
0	1	0	1
1	0	1	1
1	1	1	0

T :-

D \ Q	$\bar{Q}$	Q
$\bar{D}$		1
D	1	

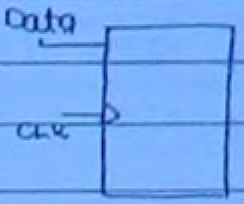
$$T = D\bar{Q} + \bar{D}Q.$$



* latch	Flip Flop.
⇒ level triggered	⇒ Edge triggered.
⇒ Asynchronous ckt	⇒ Synchronous ckt.
	

⇒ Setup time :-

The min. time required to keep I/P at proper level before ~~ally~~ apply clock.



Note:- Any ff we give Data first th ~~the~~ we apply clk.

⇒ Hold time:-

The min. time required to keep I/P is same level after applying clock.

☆ REGISTER :-

⇒ Register are used to store group of bits.

⇒ To store n bit n FF are cascaded in register.

⇒ Register are four type (Depending on I/P and O/P) :-

(i) SISO (serial in serial out).

(ii) SI PO (most imp).

(iii) PISO

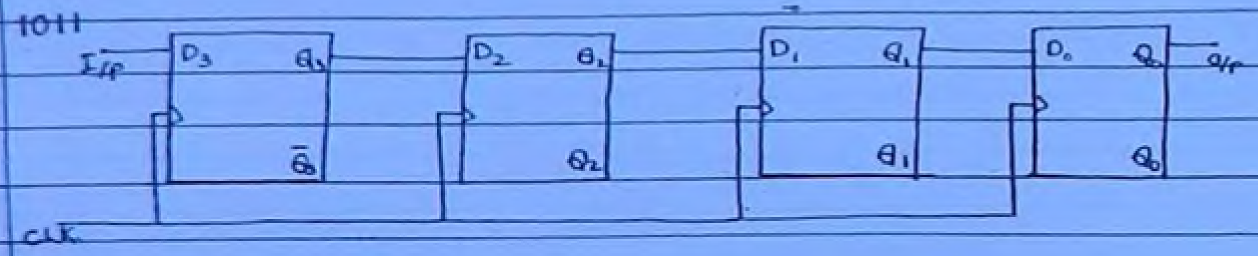
(iv) PI PO

⇒ Depending on application the register are two type:-

(i) shift register

(ii) storage register.

(A) SISO (Serial in Serial out) :-



Data	Q_3	Q_2	Q_1	Q_0	CLK.
101~~0~~1	0	0	0	0	0
	1	0	0	0	1
	1	1	0	0	2
	0	1	1	0	3
	1	0	1	1	4

⇒ For serial in register the n bit data storage requires n clock pulse.

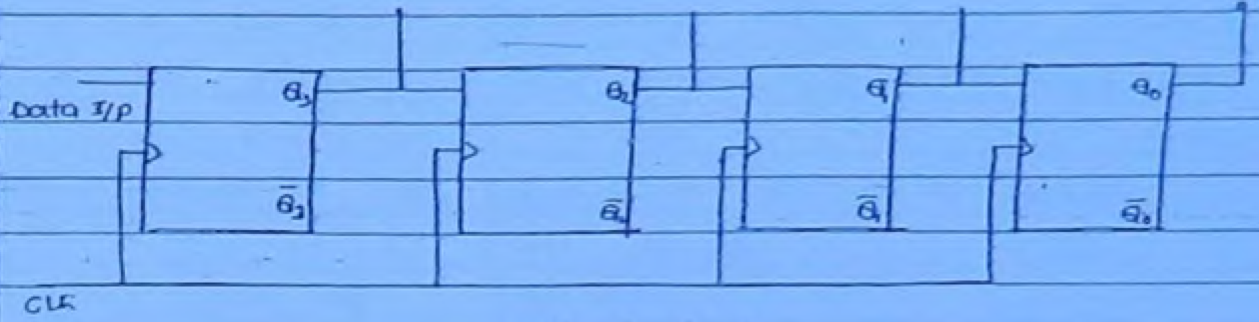
⇒ In SISO register to store n bit data is require n clock pulse.

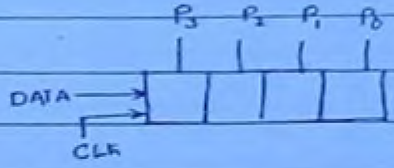
⇒ SISO register used to provide n clock pulse delay to I/P data.

$$\boxed{delay = n\,T_{CLK}}$$

⇒ To provide n bit data serially out it requires (n-1) clock pulse.

(B) SIPO (Serial in parallel out) :-





⇒ In SIPO register to provide n bit data serially in it requires n clock pulse and provide parallel o/p it requires 0 clk pulse required.

⇒ It is used to serial to parallel converter.

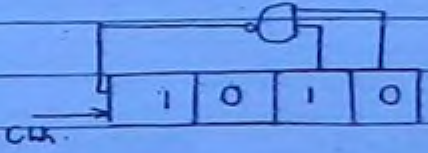
⇒ SIPO is used to convert Temporial code to spacial code.

⇒ Slow to fast converter.

serial . t =

Parallel = Spacial code.

Q:- The ckt shown in the fig. if 4 bit SIPO register which in initially loaded with 1010. If ~~stare~~ three clk pulses applied then the data if the system is. ⇒



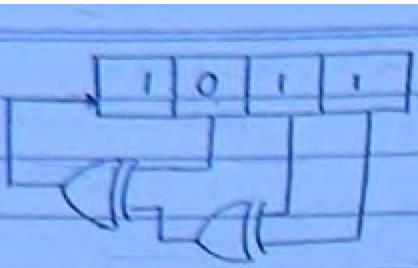
(a) 1010

(b) 1101

[✓ (c) 1111]

~~(d) 0000~~

Q:-



(a) 4
✓(b) 7
(c) 11
(d) 15

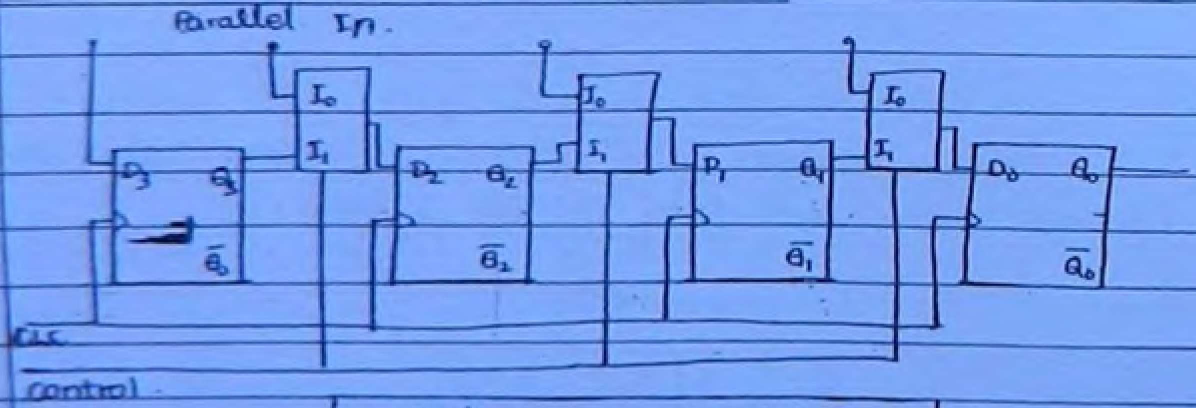
1/10

Initially loaded 1011. if clk pulse applied continuously after how many clk pulse again the data become 1010.

Sol: O/P of 3 variable X-OR is 1 if no. of 1's. is odd.

CLK	Q_3	Q_2	Q_1	Q_0
1	0	1	0	1
2	0	0	1	0
3	1	0	0	1
4	1	1	0	0
5	1	1	1	0
6	0	1	1	1
7	0	0	1	1 ✓ after 7-clock
8	0	0	0	1
9	1	0	0	0
10	0	1	0	0
11	1	0	1	0

(c) PISO (Parallel in serial out) :-



control = 0	=	Parallel In
Control = 1	=	Serial out

⇒ In PISO register to provide parallel in it require 1 clock pulse and to provide ~~pa~~ serial out (n-1) clock pulse.

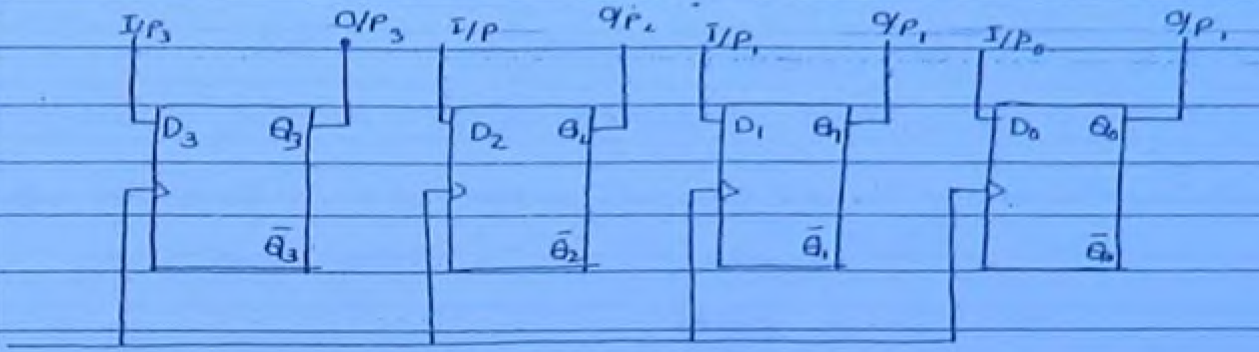
⇒ PISO is also used to convert spacial code to temporial code.

(D) PIPO (Parallel in parallel out) :-

⇒ PIPO is used as storage register.

⇒ for Parallel in it requires 1 clock pulse.

⇒ for parallel out it requires 0 clock pulse.



Important :-

	I/P	O/P
SISO	n	n-1
SIPO	n	0
PISO	1	n-1
PIPO	1	0

⇒ Each shift left register operation provide multiplication by 2.

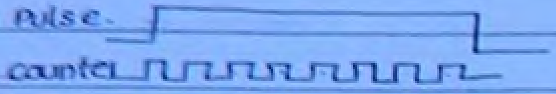
⇒ If n shift left operation ~~per~~ performed then data is multiplied by 2^n.

⇒ Each shift right operation performed then data is divide by 2.

⇒ If n shift right operation performed then data is divided by 2^n.

☆ COUNTERS :-

⇒ Counters are basically used to count no of clock pulse applied. it can also be used for frequency divider, & time measurement, frequency measurement, Range measurement, pulse width.



16× Pulse width = Total width.

⇒ Also used for waveform generator.

⇒ With n-ff, max. possible stage in the counter is 2^n.

$$\boxed{N \le 2^n}$$

or, $n \ge \log_2 N$.

where N = no. of stage

n = no. of FF.

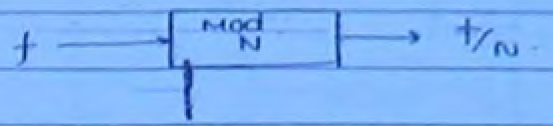
Depending on clock pulse applied counters of two type:-

(i) Asynchronous

(ii) Synchronous.

Asynchronous	Synchronous
1. Different FF are applied with different clock.	1. All FF are applied same clock.
2. It is slower.	2. It is faster
3. Fixed count sequece ie. up or down.	3. Any count sequence is possible
4. Decoding errors will present	4. No decoding error. will present.
5. Ripple counter	5. Ring counter

⇒ No. of stage use in counter mean modulus of counter
i.e. if MOD 5 counter = 5 stage.
MOD n counter = n stage



Q:- A decade counter is applied with frequency of 10MHz then O/P frequency is ...

Sol:- $f_{out} = \frac{f_{in}}{10} = \frac{10\,MHz}{10} = 1\,MHz$

⇒ Let Mod M and MOD N are cascaded then it will act as MOD MN counter.

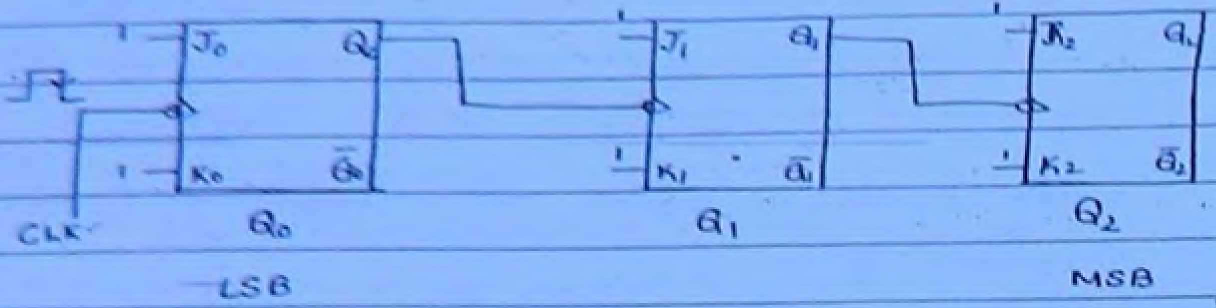
Content :-

Basic
Ripple counter
Non binary ripple counter
Ring counter
Johnson counter
Synchronous series carry
Synchronous parallel carry
Synchronous counter design and Analysis

(A) Ripple counter :-

⇒ It is a Asynchronous counter.
⇒ Different FF used different clock pulse.
⇒ Toggle mode.
⇒ Only one FF is applied with external clk and other ff's are clk is from previous ff O/P. (whether Q or $\bar{Q}$).
⇒ The FF applied with external clk will acts as LSB bit

3 bit ripple counter :- (up counter)



e) Explanation :-

⇒ The ckt shown in fig. Q_0 toggle for every clk pulse

⇒ Q_n change when Q_{n-1} change from 1 - 0. i.e. Q_2 changes when Q_1 changes from 1-0.

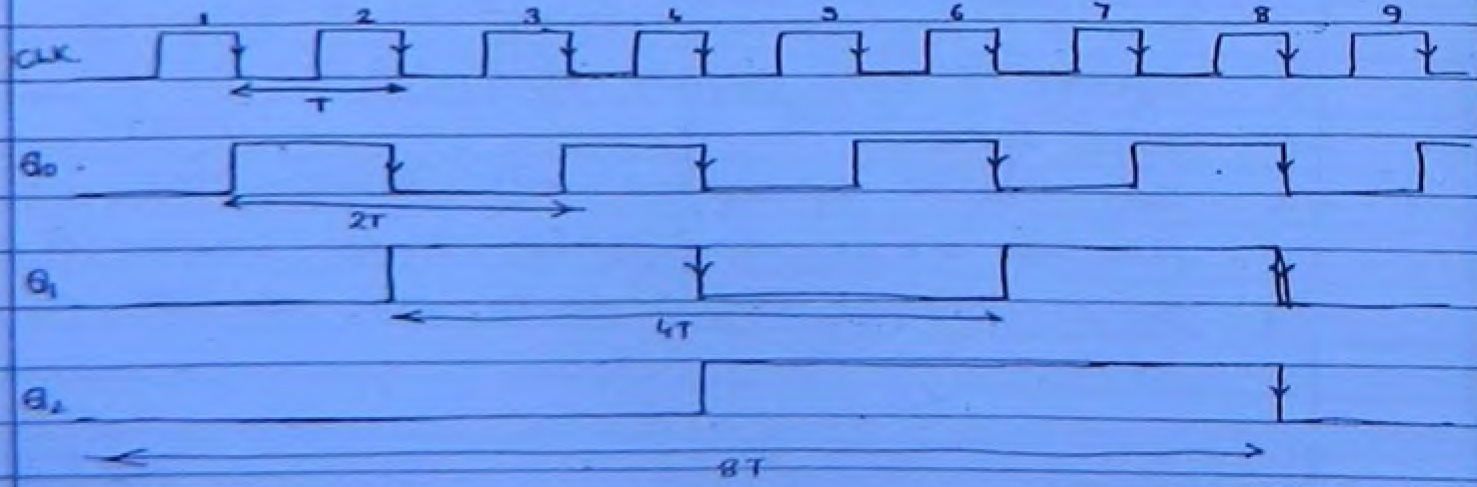
(ii) ⇒ Truth table :-

CLK	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2.	0	1	0
3.	0	1	1.
4	1	0	0
5	1	0	1
6.	1	1	0
7.	1	1	1
8.	0	0	0

⇒ This is up counter.

⇒ It is also called MOD 8 ripple counter.

(iii) Timing Diagram :-



⇒ In n bit ripple counter propogation delay of each ff is t_{Pdff} then time period of CLK is,

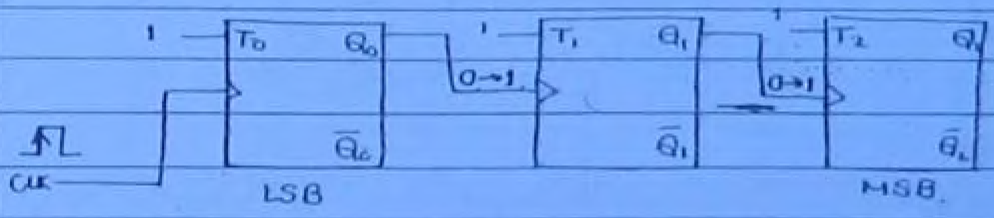
$$\boxed{\begin{array}{l} T_{CLK} \geq n\, t_{Pdff} \\ f_{CLK} \leq \dfrac{1}{n\, t_{Pdff}} \end{array}}$$

$$\boxed{f_{max} = \frac{1}{n\, t_{pdff}}}$$

Note :-

(i) -ive edge trigger → Q as clock → up counter
(ii) +ive " " → $\bar{Q}$ as clock → up counter
(iii) -ive " " → $\bar{Q}$ as clock → down counter
(iv) +ive " " → Q as clock → down counter

3-Bit Ripple counter (Down counter) :-



(i) Explanation :-

⇒ The ckt shown in fig. Q_0 toggles for every clock pulse.
⇒ Q_1 toggles when Q_0 changes from 0 to 1.
⇒ Q_2 toggles when Q_1 changes from 0 to 1.

(ii) Truth table :-

Clock	Q_2	Q_1	Q_0
0	0	0	0
1	1	1	1
2.	1	1	0
3.	1	0	1
4.	1	0	0
5.	0	1	1
6.	0	1	0
7	0	0	0

⇒ This is called ripple counter. because the input clock is the o/p of previous FF output. this is just like ripple. then called Ripple counter.

⇒ if the o/p is (000) and clock is applied then t_{pdf} is delay

000

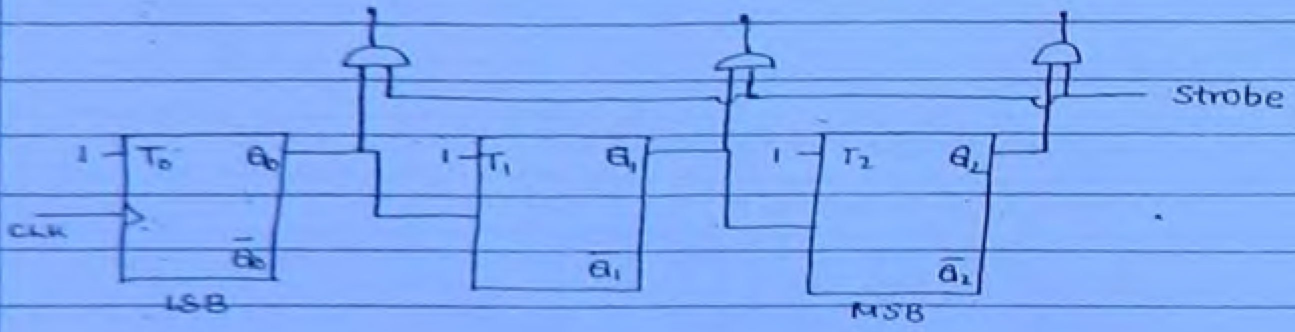
t_{pdf} → { 001 } unwanted or decoding error.

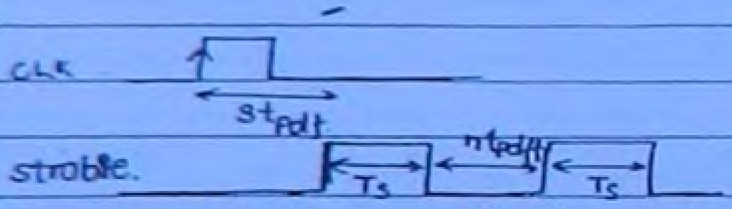
t_{pdf} → { 011 } also called transient state.

111

⇒ Decoding errors or transient state present in ripple counter due to propogation delay.

⇒ To avoid decoding error strobe signal is used.





⇒ i.e. strobe signal is zero for nt_{pdff} and after that it is one for next clock. then all the o/p is zero for the transient time therefore due to strobe signal we can remove decoding error.

$$\boxed{T_{CLK} \geq nt_{pdf} + T_S}$$

⇒ In ripple counter with n ff max. possible state is 2^n.

⇒ frequency after n 3FF in the Ripple counter is $f/2^n$ ∴ (ie. for 3FF o/p is $f/8$)

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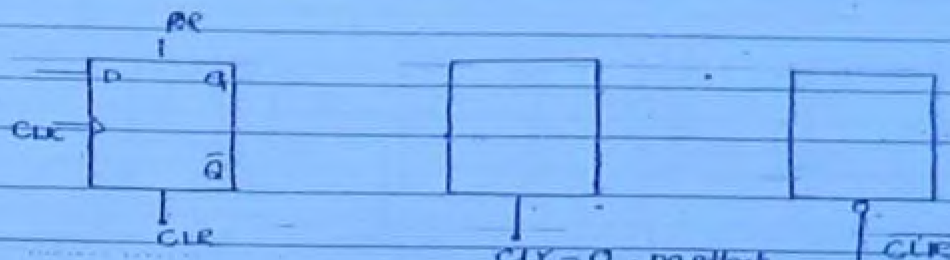
⇒ Clear and preset are known as Asynchronous I/P.

S, R, J, K, D, T are Synchronous I/p.

Clear :- clear is use to rest our ff. or counter.

Preset :- preset is use to set our FF or counter.



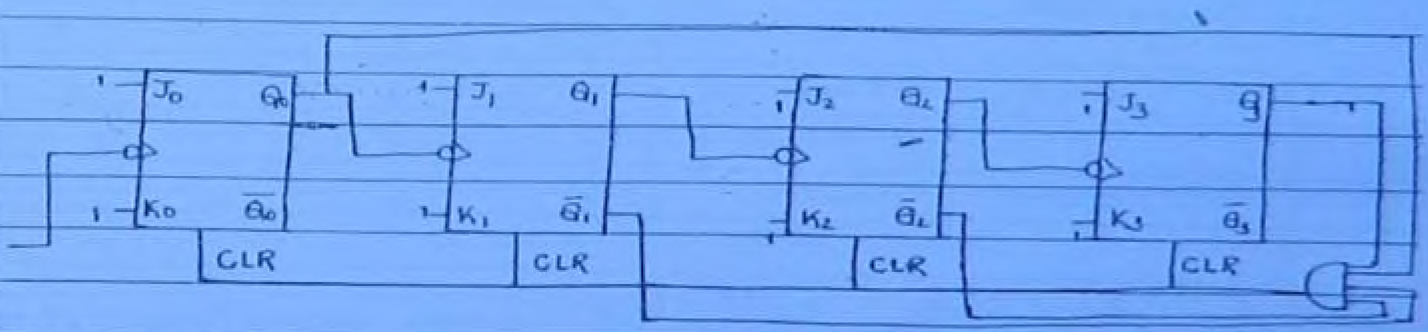
CLr = 0, no effect
= 1, ff is zero

$\overline{CLR}$ = 0 FF is zero
= 1 no effect

(B) Non Binary Ripple counter :-

(B₁) BCD counter :- (Decade counter)

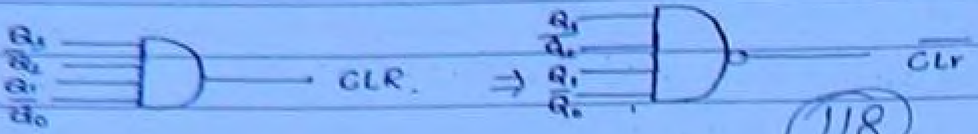
⇒ 4 flip flop used.



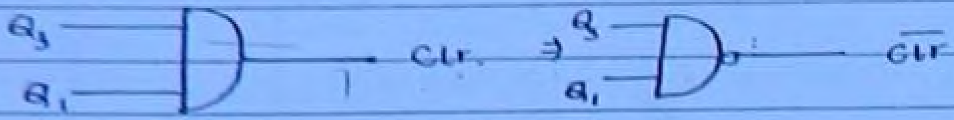
CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
0	0	0	0	0

(1010)

$Q_3\bar{Q}_2Q_1\bar{Q}_0$



if we use only Q_3 and Q_1 ,we also use this as clear ckt.



⇒ All BCD counter is Decade counter but reverse is not true.

⇒ BCD counter is Asymmetric o/p time Diagram.

⇒ o/p frequency of BCD counter is f/10.

⇒ low for 8 clock and high for 2 clock in Q_3.

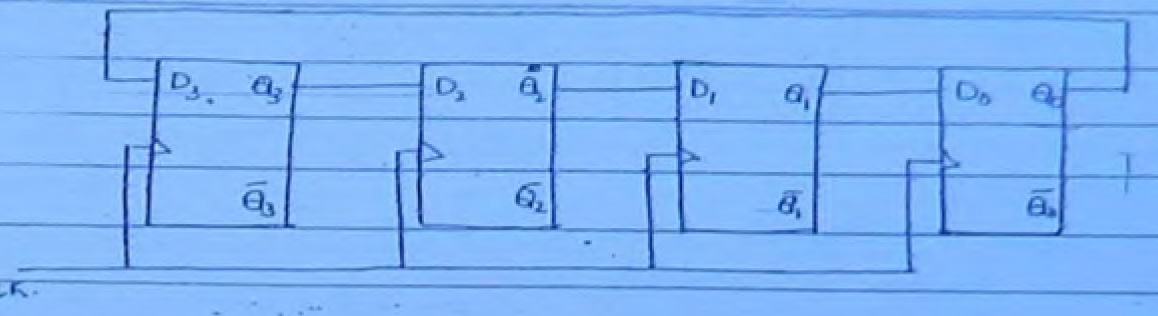
⇒ duty cycle is 20%.

⇒ In Asynchronous counter follow steps:-

1. Trigger → +ive
   → -ive
2. clock → Q
   → $\overline{Q}$
3. counter → UP
   → Down.
4. Preset /clear $\xrightarrow{\text{clear}}$ 000
   $\xrightarrow{\text{Preset}}$ 111
5. Decoding logic (Terminating logic).

(c) Ring Counter :- (Synchronous counter)

⇒ The last ff o/p is connected to first ff I/P.



(i) Explanation:-

⇒ Only one FF O/P is high and remaining FF are low.

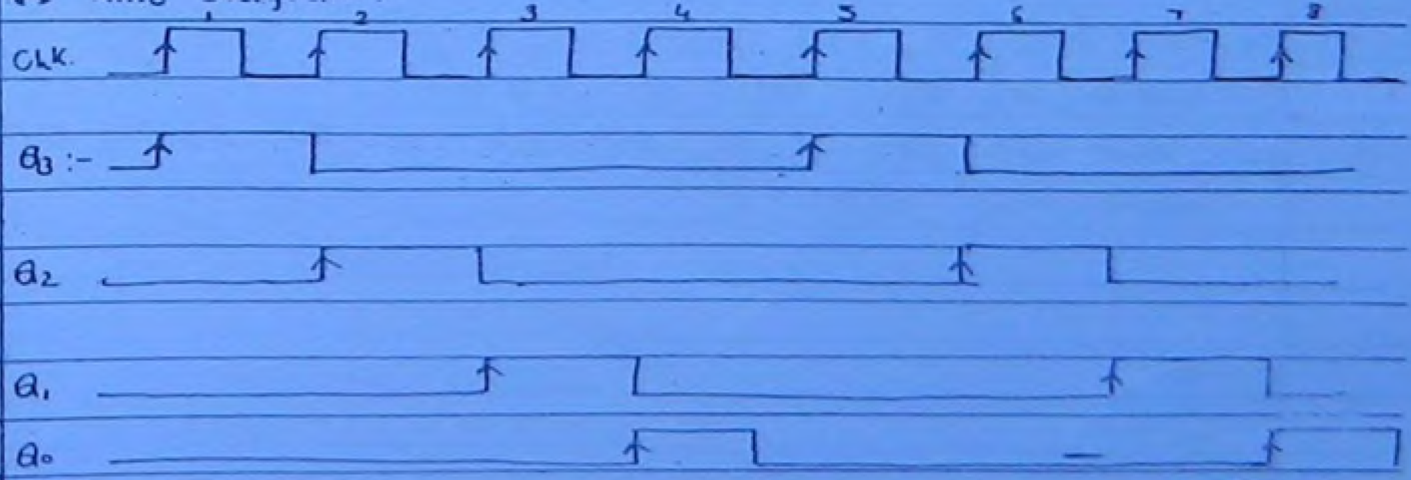
⇒ In 4 bit ring counter 4 states are there. (i.e. For n FF there is n states).

(ii) Truth table :-

CLK	Q_3	Q_2	Q_1	Q_0	
0	0	0	0	0	
1	1	0	0	0	4-state.
2	0	1	0	0	
3	0	0	1	0	
4.	0	0	0	1	
5.	1	0	0	0	

⇒ In synchronous counter the +ive edge or -ive edge. the O/P remains same.

(iii) Time Diagram :-



$\Rightarrow$ | n bit $\Rightarrow$ n state
$\Rightarrow f_0 = f/n$

(120)

$\Rightarrow$ Phase shift b/w generated waveform is 360/n.

$$\boxed{\phi = \frac{360}{n}}$$

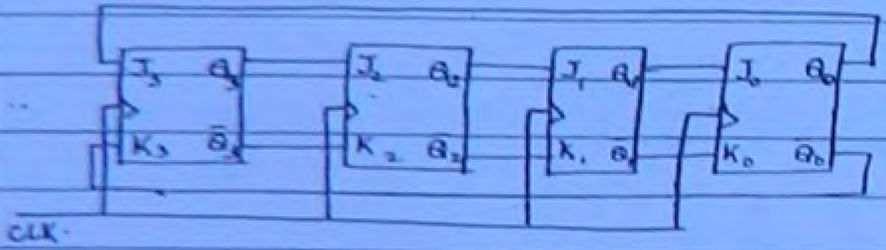
Application :-

$\Rightarrow$ used in stepper motor control.

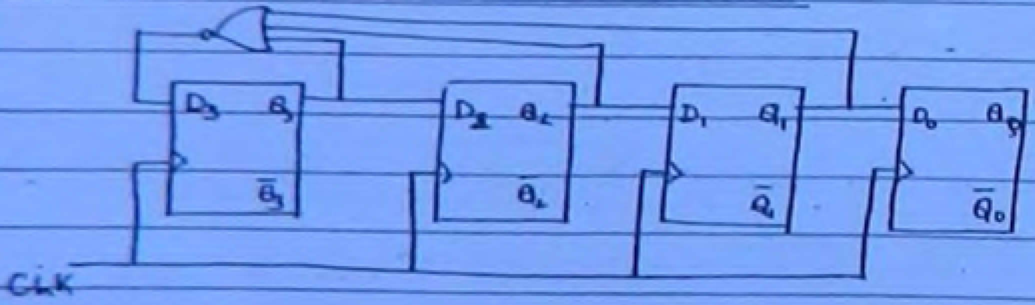
$\Rightarrow$ in Analog to Digital convertor

$\Rightarrow$ No. of unused state in ring counter is $2^n - n$.

ring counter using J-K :-



* self starting Ring counter :-

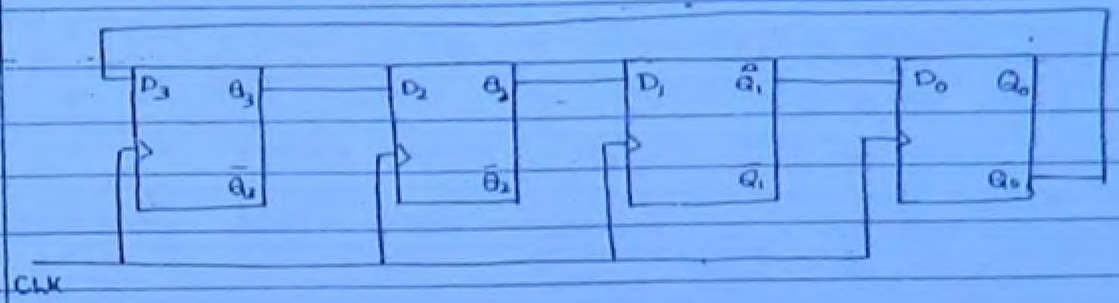


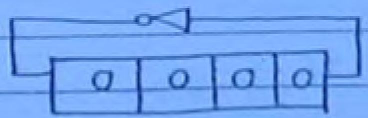
$\Rightarrow$ Advantage of Ring counter is decoding is simple. to decode no logic gate are required.

$\Rightarrow$ Last o/p can not be connected in the I/P of self start ring counter.

(D) Johnson Counter :-

- ⇒ Symmetric o/p waveform.
- ⇒ 8-stages are there for 4 bit counter.
- ⇒ phase shift = $\frac{360}{4}$ = 90°
- ⇒ It is just like SISO register.





(ii) Truth Table :-

CLK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	1	0	0	0
2	1	1	0	0
3	1	1	~~0~~1	0
4	1	1	1	1
5	0	1	1	1
6	0	0	1	1
7	0	0	0	1
8	0	0	0	0

8 state

- ⇒ Total no. of used state = 8
- ⇒ Total no. of unused state = $2^n - 8 = 2^4 - 8 = 8$ state
- ⇒ Also called Twisted ring counter, Mobies counter or, creeping counter or, Walking counter or, switch tail counter.

CLOCK	Q_3 Q_2 Q_1 Q_0		
0	0 0 0 0	→	$\bar{Q}_3 \bar{Q}_0$
1	1 0 0 0	→	$Q_3 \bar{Q}_2$
2	1 1 0 0	→	$Q_2 \bar{Q}_1$
3	1 1 1 0	→	$Q_1 \bar{Q}_0$
4	1 1 1 1	→	$Q_3 Q_0$
5	0 1 1 1	→	$\bar{Q}_3 Q_2$
6	0 0 1 1	→	$\bar{Q}_2 Q_1$
7	0 0 0 1	→	$\bar{Q}_1 Q_0$
8	0 0 0 0		

⇒ In Johnson counter to decode each state one two I/P. AND / NOR gate used.

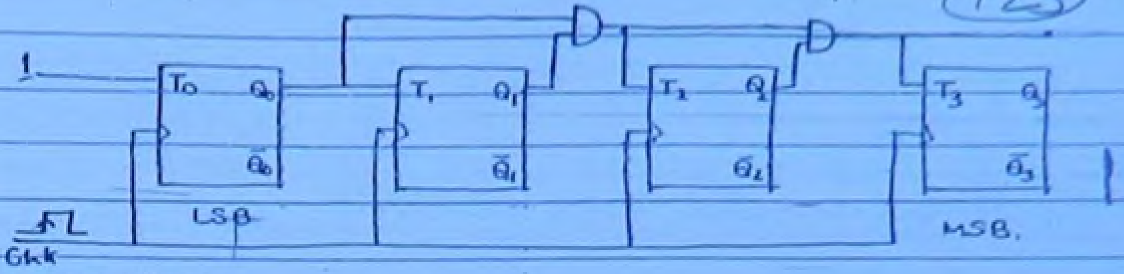
Disadvantage:

⇒ lock out may occur. (when counter enter into unused state)

Note:- In synchronous counter propagation delay of each counter is t_{pdff} then.

$$\left.\begin{array}{l} \boxed{T_{CLK} \geq t_{pdFF}} \\ \\ f_{CLK} \leq \dfrac{1}{t_{pdff}} \\ \\ \boxed{f_{max} = \dfrac{1}{t_{pdff}}} \end{array}\right\} \text{In synchronous counter.}$$

(A) Synchronous Series carry counter :-



(i) Explanation :-

⇒ ckt shown in fig. is synchronous series carry up counter.

⇒ In this counter Q_0 toggles for every clock pulse.

⇒ Q_1 toggles when $Q_0 = 1$ and clock is applied.

⇒ Q_2 toggles when $Q_1 = Q_0 = 1$ and clock applied

⇒ Q_3 will toggles when $Q_2 = Q_1 = Q_0 = 1$ and clock applied.

⇒ This ckt may be down counter when $\bar{Q}$ is connected to T.

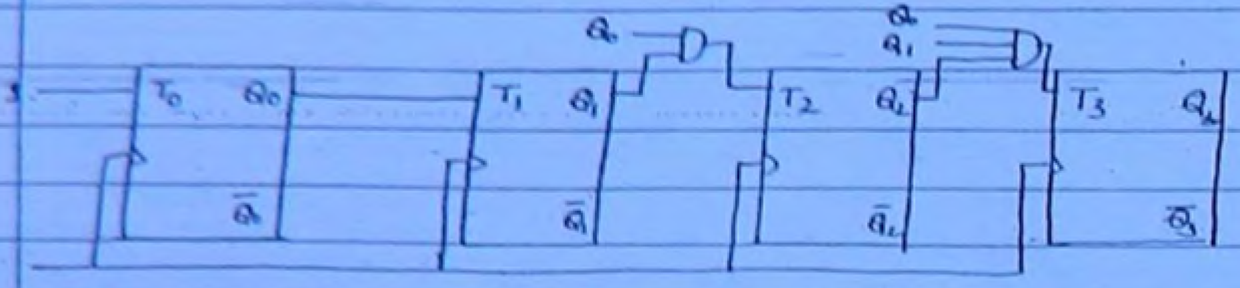
(ii) Truth table :-

CLOCK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

⇒ To provide down counter used $\bar{Q}$ o/p to provide next stage I/P.

$$\boxed{T_{CLK} \geq t_{PdFF} + (n-2)\, t_{PdAND}}$$

(B) Synchronous parallel carry counter :-



⇒ Faster than series carry counter.

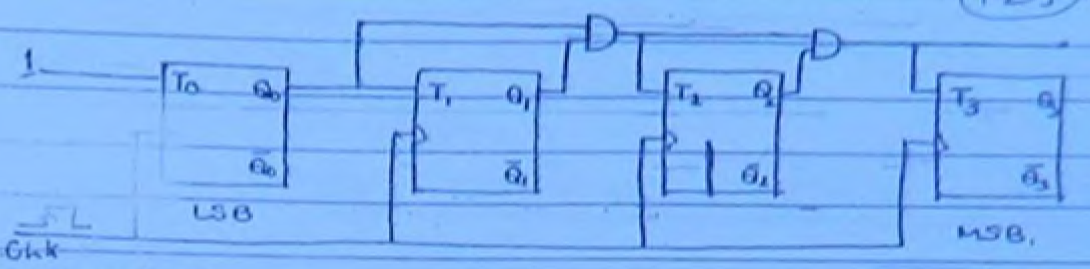
⇒ Disadvantage is increased I/P pin of AND Gate.

$$\boxed{T_{CLK} \geq t_{PdFF} + t_{PdAND}}$$

⇒ Sync

⇒ Ripple counter < Synchronous serial carry < Synchronous parallel carry counter for faster logic.

(A) Synchronous Series carry counter :-



(i) Explanation :-

⇒ ckt shown in fig. is Synchronous series carry up counter.

⇒ In this counter Q_0 toggles for every clock pulse.

⇒ Q_1 toggles when $Q_0 = 1$ and clock is applied.

⇒ Q_2 toggles when $Q_1 = Q_0 = 1$ and clock applied

⇒ Q_3 will toggles when $Q_2 = Q_1 = Q_0 = 1$ and clock applied.

⇒ This ckt may be down counter when $\bar{Q}$ is connected to T.

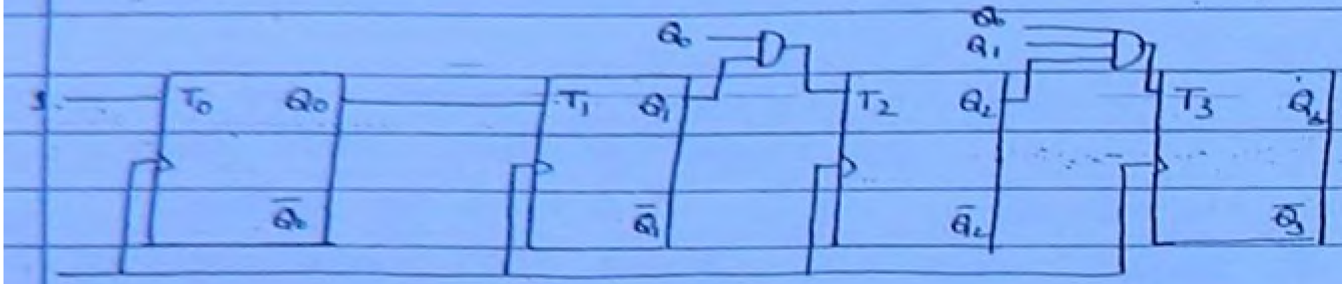
(ii) Truth table :-

CLOCK	Q_3	Q_2	Q_1	Q_0
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

⇒ To provide down counter used $\bar{Q}$ o/p to provide next stage I/P.

$$\boxed{T_{CLK} \geq t_{PdFF} + (n-2)\, t_{PdAND}}$$

B) Synchronous parallel carry counter :-



⇒ Faster than series carry counter.

⇒ Disadvantage is increased I/P pin of AND Gate.

$$\boxed{T_{CLK} \geq t_{PdFF} + t_{PdAND}}$$

⇒ Same

⇒ Ripple counter < Synchronous serial carry < Synchronous parallel carry counter for faster logic.

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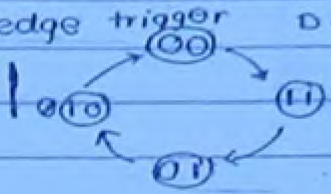
Synchronous counter design for the given sequence:-

Problem:- Design a synchronous counter for the count sequence 0→3→1→2→0 using +ive edge trigger D-FF.



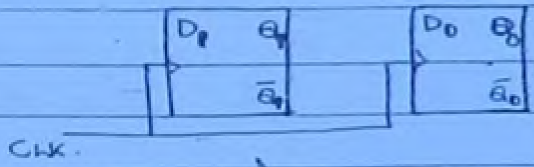
STATE DIAGRAM.

Sol:- Procedure :-

- (i) Identify no. of FF and I/p and o/p.
- (ii) construct state table.
- (iii) logical expression for I/P.
- (iv) Minimize.
- (v) Implement the ckt.

Now,

(i)



(ii) State table :-

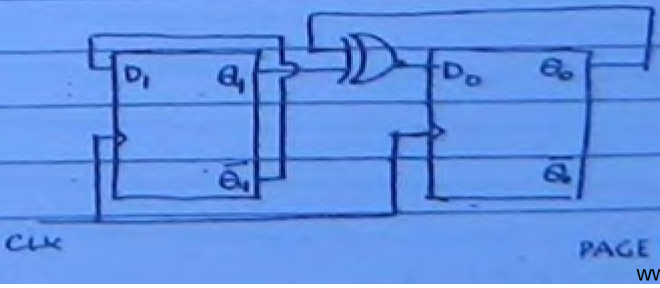
Present state	Next state	
Q_1 Q_0	Q_{1+} Q_{0+}	D_1 D_0
0 0	1 1	1 ~~0~~ 1
1 1	0 - 1	0 1
0 1	1 0	1 0
1 0	0 0	0 0

(iii) logical expression :-

$$D_1 = \bar{Q}_1\bar{Q}_0 + \bar{Q}_1 Q_0 = \bar{Q}_1 (Q_0 + \bar{Q}_0) = \bar{Q}_1$$

$$D_0 = \bar{Q}_1\bar{Q}_0 + Q_1 Q_0 = Q_1 \oplus Q_0 = Q_1 \odot Q_0$$

(iv) Implementation :-



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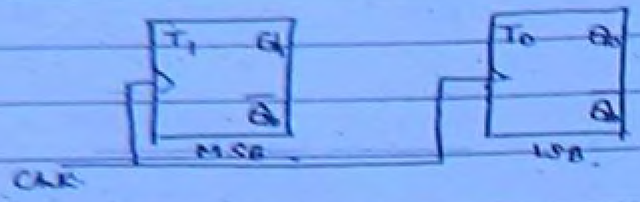
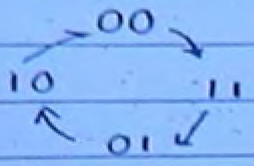
Q: Design usin T-FF. 0-3-1-2-0.

Sol:- (i)





(ii) state table.

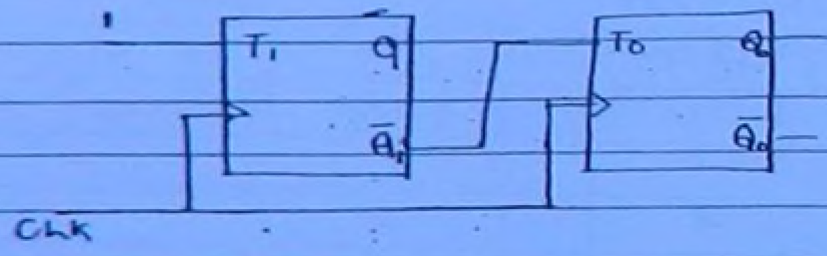
Q_1 Q_0	Q_{1+} Q_{0+}	T_1	T_0
0 0	1 1	1	1
1 1	0 1	1	0
0 1	1 0	1	1
1 0	0 0	1	0

(iii) logical expression:

$T_1 = 1$

$T_0 = \bar{Q}_1\bar{Q}_0 + \bar{Q}_1 Q_0 = \bar{Q}_1$

(iv) Implementation:-



Content :-

- ⇒ Various no. system.
- ⇒ Arithmetic operation.
  - → complement
  - → Add , sub.
- ⇒ Various codes.
- ⇒ Data representation.
  - → unsigned
  - → signed
    - → signed magnitude
    - → 1's
    - → 2's

Number system and codes :-

- Weighted
  - ⇒ Positional weighted
  - e.g. Binary , octal
    Decimal , Hexdecimal
    BCD code.
- Unweighted.
  - ⇒ No weighted
  - e.g. gray code , Excess -3 code

⇒ A number system with base or radix r contains , r different digit and they are from (0— r-1).

e.g. $(101)_r$

r = Base or radix.

Base	Different Digit.
2	0, 1
8	0, ... 7
10	0, - - - 9
12	0, --- 9, A, B
16	0, 9, A, B, C, D, E, F
4	0 , - - - 3
6	0, 1, 2, 3, 4, 5

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☆ Conversion (various number system) :-

1. Decimal to others :-

⇒ To convert decimal no. into any other base r divide integer part multiply fractional part with r.

e.g.

Q:- convert $(25.625)_{10}$ — $(—)_2$.

Sol^n:-

2 | 25
2 | 12 − 1 ↑
2 | 6 − 0
2 | 3 − 0
2 | 1 − 1
   0 − 1

0.625 × 2 = 1.25 = 1. ↓
0.25 × 2 = 0.50 = 0
0.5 × 2 = 1.0 = 1

Ans :- $(11001.101)_2$

Q:- Convert (25.625) — $(—)_8$.

Sol^n:-

8 | 25
8 | 3 − 1 ↑
   0 − 3

0.625×8 = 5.

Ans :- $(31.5)_8$.

⇒ When we go from higher to lower base the no. + is increased.

Q:- convert $(26.625)_{10}$ — $(—)_{16}$

Sol^n:-

16 | 25
16 | 1 − 9 ↑
   0 − 1

0.625×16 = 10. = A

Ans :- $(19.A)_{16}$.

Q: convert $(254)_{16}$ — $(—)_{16}$.

Sol^n:

16 | 254
16 | 15   14 = E ↑
   0   15 = F

= $(FE)_{16}$

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Q: Convert $(27.4)_{10}$ — $(-)_4$

Sol:

$$\begin{array}{r|l} 4 & 27 \\ 4 & 6 - 3 \\ 4 & 1 - 2 \\ & 0 - 1 \end{array} \uparrow$$

$0.4 \times 4 = 1.6 = 1$
$0.6 \times 4 = 2.4 = 2$
$0.4 \times 4 = 1.6 = 1$ ↓

Ans:- $(123.\overline{12}1)_4$

2: Others to Decimal :-

$$(x_1 x_2 x_3 . Y_1 Y_2)_r = (\quad)_{10}$$

⇒ To convert any other base r to decimal multiply each digit with positional weighted then add.

then,

$$(—)_{10} = x_1 \times r^2 + x_2 r^1 + x_3 \times r^0 + Y_1 r^{-1} + Y_2 r^{-2}$$

Q:- Convert $(10101.11)_2 = (—)_{10}$.

Sol: $1 \times 2^4 + 0 \times 2^3 + 1 \times 2^2 + 0 \times 2^1 + 1 \times 2^0 + 1 \times 2^{-1} + 1 \times 2^{-2}$

$= 16 + 4 + 1 + \frac{1}{2} + \frac{1}{4}$

$= \frac{64 + 16 + 4 + 2 + 1}{4} = \frac{87}{4} = (21.75)_{10}$

Q:- convert $(57.4)_8 = (\quad)_{10}$

Sol:- $5 \times 8^1 + 7 \times 8^0 + 4 \times 8^{-1}$

$= 40 + 7 + \frac{4}{8} = \frac{320 + 56 + 4}{8} = \frac{380}{8}$

$= 47.5 = (47.5)_{\cancel{8}10}$

Q:- convert $(57.4)_{16} = (\quad)_{10}$.

Sol: $5 \times 16 + 7 + \frac{4}{16} = 87 + 0.25 = (87.25)_{10}$

Q:- Convert $(BAD)_{16} = (\quad)_{10}$

Sol:- $11 \times 16^2 +$ ~~AX1~~ $10 \times 16 + 13$

$= 256 \times 11 + 160 + 13$

$= 2816 + 160 + 13 = (2989)_{10}$.

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Q:- convert $(35)_6 = (-)_{10}$

Sol:- $3\times6 + 5\times1 = 18+5 = (23)_{10}$

3. Octal to Binary & Binary to Octal :-

$(xyz)_8 = (-)_2$

⇒ each no. is represent by its 3 bit binary formate.

Ques:- convert $(37.45)_8 = ( )_2$

Sol:- $(011111 . 100101)_2$

Binary to octal :-

Ques:- convert $(10110.11)_2$

Sol:- $(010\ 110 . 110)_2$

$= (26.6)_8$.

4. Hexadecimal to Binary and Binary to Hexadecimal :-

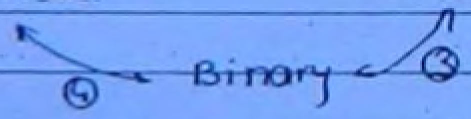
⇒ Each digit is represent by 4 bit binary.

Ques:- convert $(259A)_{16} = (-)_2$

Sol:- $(0010\,0101\,1001\,1010)_2$

5. Hexadecimal to octal or octal to Hexa :-

for Hexa ←——→ Octadecimal



Q: convert $(CAD)_{16} = ( )_8$

Sol:- $(CAD)_{16}$

$= (\underbrace{110}\underbrace{010}\underbrace{101}\underbrace{101})_2$

$= (6255)_8$

☆ ARITHMETIC OPERATION :-

(A) Binary Addition, subtraction, Multiplication :-

Q: Add

$$\begin{array}{r} 110110 \\ +\,101101 \\ \hline 1100011 \end{array}$$

Q: Sub :-

$$\begin{array}{r} 11\overset{2}{0}11 \\ 10110 \\ \hline 00101 \end{array}$$

Q. Multiply :

(a)

$$\begin{array}{r} 1010 \\ 101 \\ \hline 1010 \\ 0000 \\ 1010 \\ \hline 110010 \end{array}$$

(b)

$$\begin{array}{r} 1111 \\ 1111 \\ \hline 1111 \\ 1111 \\ 1111 \\ 1111 \\ \hline 0\,0\,0\,0\,0\,1 \\ 111 \end{array}$$

$\rightarrow 4 = \underbrace{1}\underbrace{00}$

$\rightarrow 6 = \overset{2}{\underbrace{11}_{3}}\underbrace{0}$

(B) Octal Addition, subtraction :-

0+0 = 0

0+1 = 1

1+1 = 2

1+7 = 10

7+2 = 11

$7+1 = (8)_{10} = \begin{array}{r|l} 8 & 8 \\ 8 & 1 - 0 \\ & 0 - 1 \end{array} \uparrow = (10)$

$7+7 = \begin{array}{r|l} 8 & 14 \\ 8 & 1 - 6 \\ & 0 - 1 \end{array} \uparrow = 16.$

Sum of 2 octal no:-

(i)

$$\begin{array}{r} 243 \\ +\,212 \\ \hline 455 \end{array}$$

(ii)

$$\begin{array}{r} 567 \\ +\,243 \\ \hline 1032 \end{array}$$

Q:- Subtract :-

(1)

$$\begin{array}{r} 7\overset{8}{4}3 \\ 564 \\ \hline 157 \end{array}$$

(C) Hexadecimal (Add, Subtraction) :-

Addition :-

1+1 = 2 A+A = $(20)_{10}$ = $(14)_{16}$

1+9 = A 1+B = C

Q:- (i)

```
 5 6 8 9
 4 5 7 4
 -------
 9 B F D
```

(ii)

```
 A D D
 D A D
 -----
188[illegible]A
```

16|26
16|1 - 10
1 - 1

13
7
16|24
1 - 8
11
U , 24

Q: Subtract :

Sol: (i)

```
 9 7 4 B
 5 8 7 C
 -------
 3 E C F
```

16

(ii)

```
  9654
- 5321
  4333
```

(D) Complements :-

r = → (r-1)'s complement
→ r's complement

Binary → 1's
→ 2's

Octa → 7's
→ 8's

Decimal → 9's
→ 10's

Hexa → F's
→ 16's

(r-1)'s complement :-

⇒ Subtract from max. no. to the given no.

e.g. comp. of (1010)

= 1111
1010
0101

To determine (r-1)'s compliment subtract given no from max. no. possible in the given base. (max. no. ~~[illegible]~~) $(r^n - 1)$.)

e.g. 1's complement of 101101 is,

Sol^n.-
111111
− 101101
010010

Q:- determine 7's complement of octal no. 5674.

Sol^n.-
7 7 7 7
− 5 6 7 4
2 1 0 3

Q:- Determine 9's compliment of Decimal 2679.

Sol^n:-
9 9 9 9
− 2 6 7 9
7 3 2 0

Q: Det. F's comp. of Hexa. 2689.

Sol^n
F F F F
− 2 6 8 9
− D 9 7 6

(ii) r's complement :-

To determine r's complement first write (r-1)'s complement then add 1 at LSB. (at right most)

Q:- Det. 2's complement of 10100.

Sol:

136

```
  11111
- 10100
-------
  01011
     +1
-------
  01100  Ans.
```

Q:- Determine 2's complement of 10110.11

Sol:- 1's complement = 01001.00

```
  01001.00
        +1
----------
  01001.01  Ans.
```

Q:- Determine 8's complement of octal 2670.

Sol:- 7's comp =

```
  7777
- 2670
------
  5107
    +1
------
  5110
```

Q: Determine 10's Complement of Decimal 5690.

Sol:- 9's =

```
  9999
- 5690
------
  4309
    +1
------
  4310
```

Q: Determine 16's complement of Hexadecimal 5289.

Sol:- 15's = F's =

```
  FFFF
- 5289
------
  AD76
    +1
------
  AD77
```

CODES :-

1. BCD code :-

⇒ Binary coded decimal
⇒ weighted code.
⇒ 4 bit Code.
⇒ 8421 code.
⇒ Each decimal digit with is represented with 4 bit

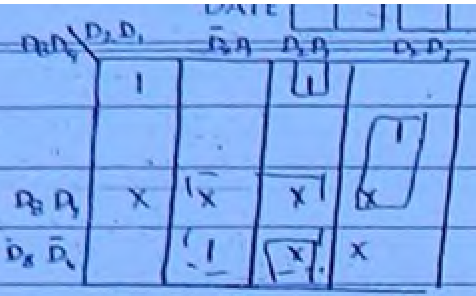
Decimal	BCD	Excess -3 code.
0	0000	0011
1	0001	0100
2	0010	0101
3	0011	0110
4	0100	0111
5	0101	1000
6	0110	1001
7	0111	1010
8	1000	1011
9	1001	1100

1010
1011
1100
1101
1110
1111
} invailid BCD code or. don't care.

⇒ During Arithemetic operation if invalid. BCD present the add 0110 to get corect result.

oblems - A combinational ckt is applied with 4bit BCD code which is represented as $D_8 D_4 D_2 D_1$, o/p is Y., Y=1 then I/p BCD is divisible by 3. then logical expressi for Y is.

Sol. 0000 - 0
0011 - 3
0110 - 6
1001 - 9 } →



$Y = \bar{D}_8\bar{D}_4\bar{D}_2\bar{D}_1 +$ ~~$\bar{D}_8\bar{D}_4\bar{D}_2 D_1 + D_8 D_1$~~
$+ D_8 D_1 + D_2 D_1 \bar{D}_4 + D_2 \bar{D}_1 D_4$

$Y = \bar{D}_8\bar{D}_4\bar{D}_2\bar{D}_1 + D_1D_8 + D_1D_2\bar{D}_4 + \bar{D}_1D_2D_4$

⇒ For write BCD code each digit (decimal) is write seperately in BCD.

e.g. $(534)_{10} = (010100110100)_{BCD}$

2. Excess - 3 code :-

⇒ Excess - 3 code = BCD + 3

⇒ Unweighted code

⇒ 4 bit code.

Decimal	Excess -3 code
0	0011
1	0100
2	0101
3	0110
4	0111
5	1000
6	1001
7	1010
8	1011
9	1100

self complement

⇒ It is self complement code.

⇒ Only unweighted code which is self complement is Excess 3-code.

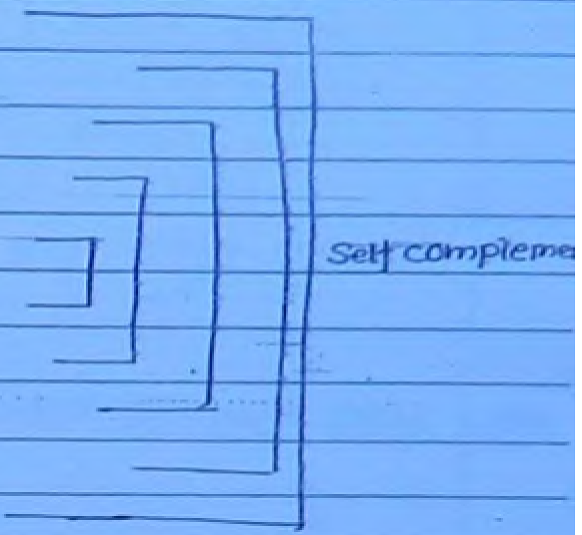
⇒ The code which addition is 9 is self complement code.

e.g. 2421
3321
4311
5211 } weighted } self complemented.

Q: Write 2421 weighted code.

Sol.

Decimal	2 4 2 1
0	0 0 0 0
1	0 0 0 1
2	0 0 1 0
3	0 0 1 1
4	0 1 0 0
5	1 0 1 1
6	1 1 0 0
7	1 1 0 1
8	1 1 1 0
9	1 1 1 1



3. Binary to Gray code :-

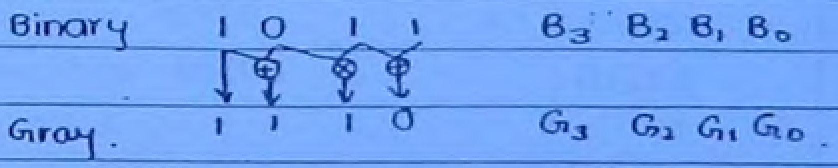
(A) Binary to Gray :-

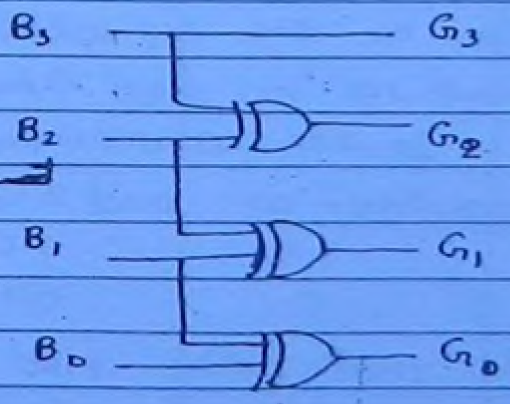
⇒ Unweighted code.

⇒ successive no. is differ by 1 bit.

⇒ Also called unit distance code.

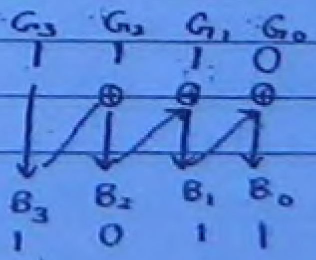
⇒ Also cyclic code, Reflective code and Minimum error code.

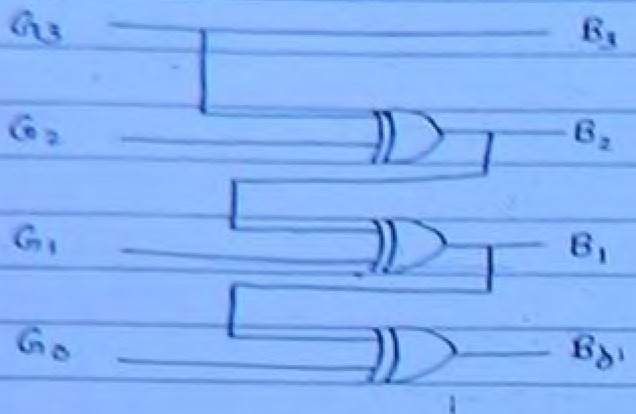




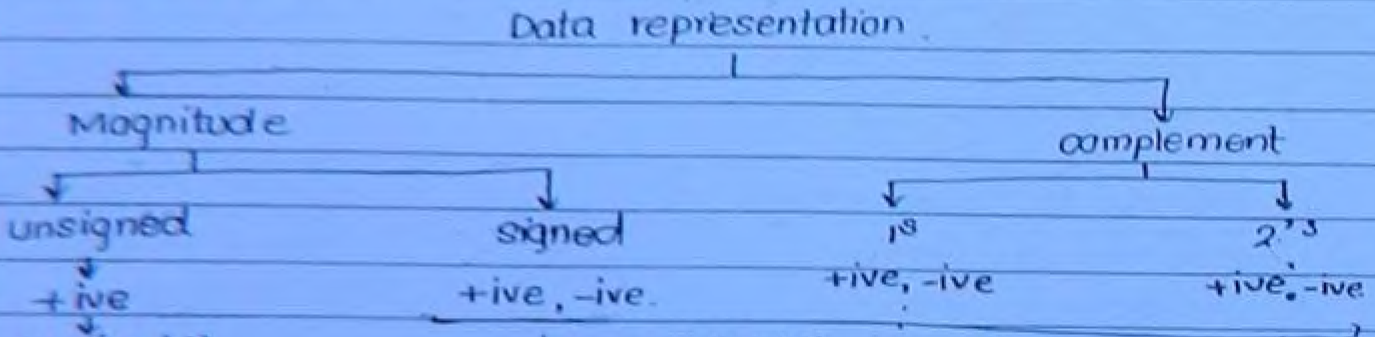
(B) Gray to Binary :-

Binar. Gray





☆ Data Representation :-



no sign bit

one extra bit → sign.

sign → MSB

logic - 0 → +ive

- 1 → -ive.

+6	110	0110	0110	0110
-6	x (can't write)	1110	1001	1010

⇒ In all representation +ive no. are represented in similar way. To represent -ive no in sign magnitude only sign bit change. In 1's complement represent of -ive no., first write positive no. and then 1's complement to it.

⇒ And in 2's complement first write +ive no. and then 2's complement to it.

Q:⇒ A no. is represent in ~~to~~ 2's complement for 1011 the equivalent decimal value.

Sol:-
$$1011 = -(0101) = -(0101)$$
$$= -5.$$

Q:- To find 5-4 ?

Sol:- 5+(-4)

+5 = 0101   +5+(-4) = 0101

-4 = 1100   1100

* 0001

⇒ In 2's complement addition if any carry present it is discarded.

⇒ In 2's complement to extend no. of bit copy MSB bit.

Q:-17. Page - (6).

Sol:- 1001 → -(0111) = -7

11001 → -(001101) = -7

111001 → -(000111) = -7.

Binary	sign mag	1's	2's
0000	+0	+0	+0
0001	+1	+1	1
0010	+2	2	2
0011	+3	3	3
0100	+4	4	4
0101	+5	+5	+5
0110	+6	+6	+6
0111	+7	+7	+7
1000	-0	-7	-8 *
1001	-1	-6	-7
1010	-2	-5	-6
1011	-3	-4	-5
1100	-4	-3	-4
1101	-5	-2	-3
1110	-6	-1	-2
1111	-7	-0	-1

4 bit :-

(i) range of signed mag $-7 \rightarrow +7$

(ii) " " 1's complement $-7 \rightarrow +7$

(iii) " " 2's complement $-8 \rightarrow +7$

⇒ For signed mag. and 1's complement :-

n bit → $-(2^{n-1}-1)$ to $+(2^{n-1}-1)$

⇒ For 2's complement :-

n bit → $-(2^{n-1})$ to $+(2^{n-1}-1)$

Q:- Perform 5+4 using 2's complement.

Sol:-

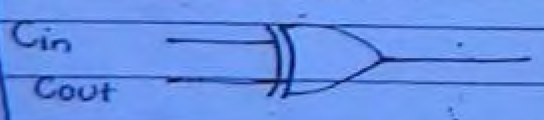
$$\begin{array}{rcl} 5 & = & 0101 \\ 4 & = & 0100 \\ \hline & & ①001 \end{array} \quad \times$$

↳ overflow may occur when same (two because sign no. are added in signed representation. because for 4 bit we can only represent

$-(2^{n-1})$ to $+(2^{n-1}-1)$ = $(-8 \rightarrow +7)$

let X and Y are sign bit of two no. and Z is resultant sign no. then condition for overflow is.

Z = $\boxed{\bar{X}\bar{Y}Z + XY\bar{Z}}$ condition of overflow.



0 – No overflow

1 – Overflow.

DATE

let Cin = carry into MSB

Cout = carry from MSB.

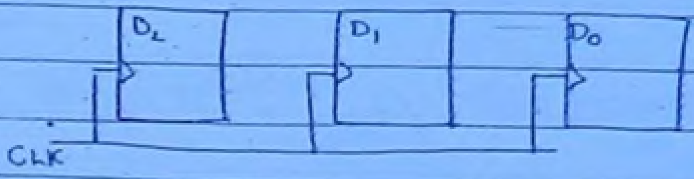
143

classmate

PAGE

Q: Design a synchronous counter using D-FF for the sequence
$0 \to 2 \to 5 \to 3 \to 4 \to 7 \to 0$.

Sol: (i)



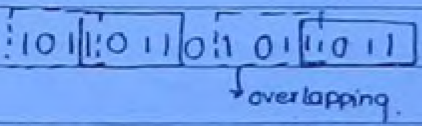
since 1,6 is unused
used lock out condition
i.e. 1 → 0
6 → 0

(ii) Truth table:-

PS			NS		
Q_2	Q_1	Q_0	Q_{2+}	Q_{1+}	Q_{0+}
0	0	0	0	1	0
0	1	0	1	0	1
1	0	1	0	1	1
0	1	1	1	0	0
1	0	0	1	1	1
1	1	1	0	0	0
0	0	1	0	0	0
1	1	0	0	0	0

⇒ To avoid lock out change unused states into one of used states in state table.

Q:- 10 or, 31.

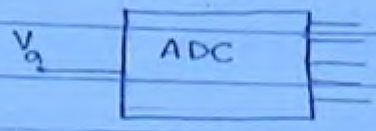


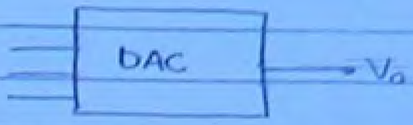
⇒ 4bit ⇒ 4 state requires ⇒ 2 FF required.

Moore & Mealy :-

State Machines

Moore	Mealy
⇒ o/p depend on present state	⇒ o/p depend on → Presents → Present i/
⇒ Design easy	⇒ Design complex.
⇒ More no. of state	⇒ less no. of state.





(a) Counter type ADC

(b) SAR type ADC

(c) Parallel comparator type

(d) dual slope integrating type.

(i) Weighted resistor

(ii) R-2R ladder.

(A) Digital to Analog converter (DAC) :-

(1) Resolution / step size.

(2) Analog o/p voltage.

(3) V_{FS} (4) % Resolution (5) Error Accuracy

1. Resolution / Step size :-

It change in analog voltage corresponding one LSB increment in the I/p.

$$\boxed{\text{Resolution} = \frac{V_r}{2^n - 1}}$$

where V_r = reference voltage corresponding to logic 1
n = no. of bits.

2. Analog o/p voltage :-

$$\boxed{V_{analog} = \text{Resolution} \times \text{Decimal equivalent of binary dat}}$$

Q1. In a 4 bit DAC reference voltage 5V. if binary data 1001 is applied then analog voltage is.

Sol:

$$\text{Resolution} = \frac{V_r}{2^n - 1} = \frac{5}{16-1} = 1/3$$

$$V_{analog} = \frac{1}{3} \times 9 = 3\text{V}.$$

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(3) V_{FS} :-

Full scale voltage is the max. o/p voltage of DAC.

$$V_{FS} = \frac{V_r}{2^n-1} \times 2^n-1$$

$$\boxed{V_{FS} = V_r.}$$

(4) % Resolution :-

$$\boxed{\% \text{ Resolution} = \frac{\text{Resolution}}{V_{FS}} \times 100.}$$

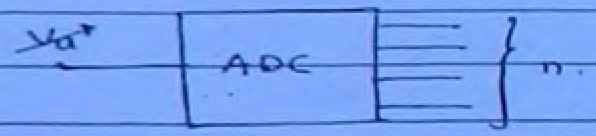
$$\boxed{\% \text{ Resolution} = \frac{1}{2^n-1} \times 100}$$

(5) Errors / Accuracy :-

⇒ Max error acceptable in ADC's or DAC's is equal to resolution or step size.

(B) Analog to Digital converter :-

Characteristics of ADC's :-



(1) $$\boxed{\text{Resolution} = \frac{\text{range}}{2^n-1}}$$

where,

$V_{range} = V_{max} - V_{min}$.

(2) $$\boxed{\% \text{ Resolution} = \frac{1}{2^n-1} \times 100}$$

(3) $$\boxed{\begin{aligned}\text{Dynamic range} &= (6n + 1.76)\,dB \\ &\approx 6n\,dB\end{aligned}}$$

Resolution of R-2R ladder type DAC's is :-

$$\boxed{\text{Resolution} = \frac{V_r}{2^n}}$$

Ques- 5. Page 41.

Sol^n -

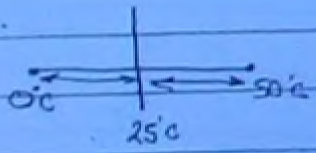
$V_{FS} = 10.24$

$n = 10$

$$\text{Resolution} = \frac{10.24}{2^{10}} = 10\text{mv}.$$

$$\text{error} = \frac{\text{LSB}}{2} = \frac{10\text{mv}}{2} = \pm 5\text{mv}$$

calibarate at 25° i.e. error at 25°c is zero.



$\Rightarrow \pm 25^\circ c \rightarrow 5\text{mV}$

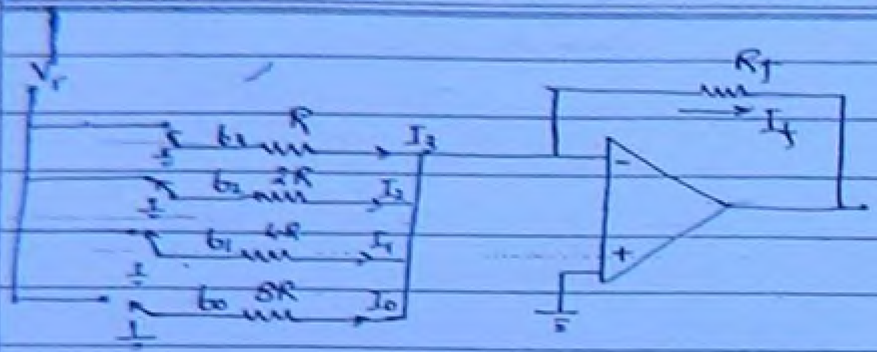
$$1^\circ C = \frac{5}{25^\circ c}\text{mV}$$

$$= 0.2\ \text{mV}/^\circ c = 200\ \mu V/^\circ c.$$

(A) Digital to Analog Circuit :-

Digital to Analog circuits :-

(A) Weighted Resistor DAC :- (4Bit) :-



b_3 = MSB = more current

b_0 = LSB = less current

$$I_3 = \frac{V_r}{R} * b_3$$

$$I_2 = \frac{V_r}{2R} * b_2$$

$$I_1 = \frac{V_r}{4R} * b_1$$

$$I_0 = \frac{V_r}{8R} * b_0$$

$$I_f = I_3 + I_2 + I_1 + I_0$$

$$V_0 = -I_f R_f$$

$$\boxed{\text{LSB resistance} = (2^{n-1}) \text{-MSB resistance.}}$$

⇒ In weighted resistor DAC the accuracy is less due to use of different resistance.

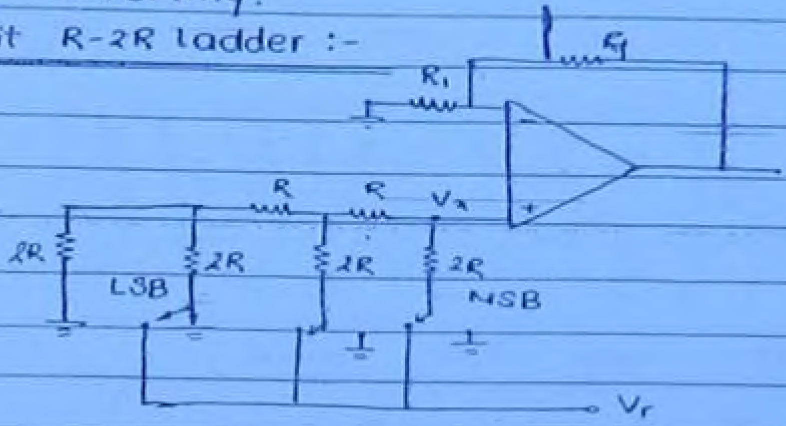
⇒ To overcome this we use R-2R ladder used.

(B) R-2R ladder :-

- Normal ladder
- Inverted ladder.

* Non inverting
* Inverting.

(B₁) 3 Bit R-2R ladder :-



⇒ Adjecent to 2R is LSB.

$$V_o = \left(1 + \frac{R_f}{R_1}\right) V_x$$

V_x = Resolution * Decimal equivalent of Binary data.

$$= \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i$$

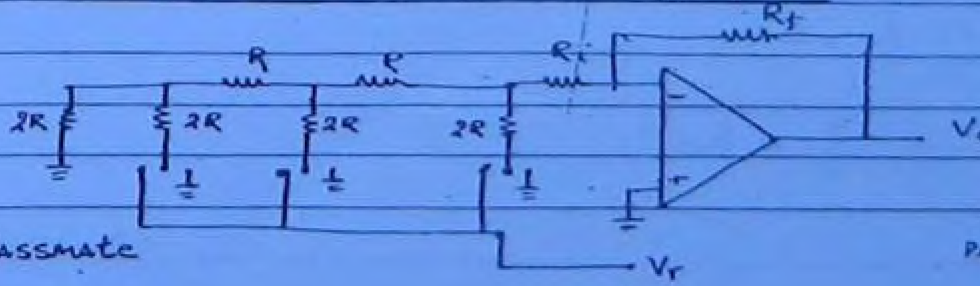
(decimal equivalent = $b_2 b_1 b_0$ (binary data))

$$= b_2 2^2 + b_1 2^1 + b_0 2^0 = \sum_{i=0}^{n-1} 2^i b_i$$

$$\boxed{V_o = \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i * \left(1 + \frac{R_f}{R_1}\right)}$$

V_o = Resolution * Decimal * gain.

(B₂) 3 Bit R-2R ladder (Inverting) :-

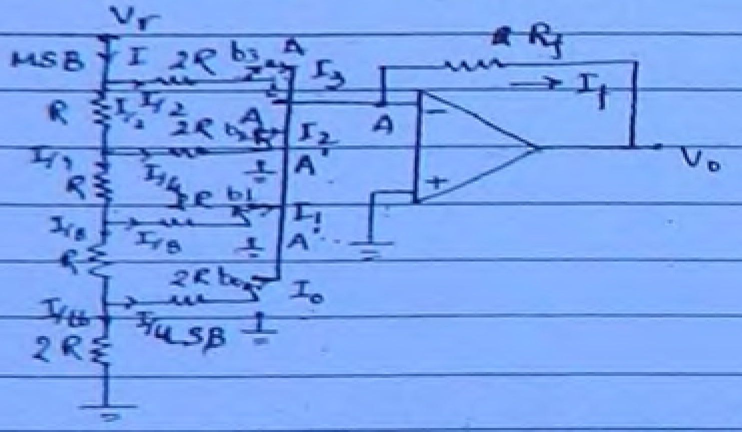


V_o = Resolution * decimal * gain.

$$\boxed{V_o = \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i * \left[\frac{-R_f}{R_1 + R}\right]}$$

$$\boxed{I_f = \frac{V_r}{2^n} * \sum_{i=0}^{n-1} 2^i b_i \times \left[\frac{1}{R_1 + R}\right]}$$

3) Inverted ladder type DAC circuit :-



⇒ Since A and A' both are ground then (logical or virtual ground and ground) the switch is at same potential then charging and discharging of switch problem removed in previous ckt.

$I = V_r/R$

$I_3 = \cancel{\frac{I/2}{b_3}} \quad \frac{I}{2} \times b_3$

$I_2 = \frac{I}{4} \times b_2$

$I_1 = \frac{I}{8} \times \cancel{I}\, b_1$

$I_0 = \frac{I}{16} \times b_0$

$I_f = I_0 + I_1 + I_2\ I_3$

$= \frac{I}{16}\left[8b_3 + 4b_2 + 2b_1 + b_0\right]$

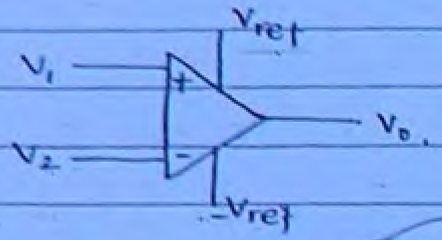
$= \frac{V_r}{2^n}\left(\sum_{i=0}^{n-1} 2^i b_i\right) \times \frac{1}{R}$ (153)

$$\boxed{I_f = \frac{V_r}{2^n}\left(\sum_{i=0}^{n-1} 2^i b_i\right)\frac{1}{R}}$$

$$\boxed{V_0 = \frac{V_r}{2^n}\left(\sum_{i=0}^{n-1} 2^i b_i\right)\left(\frac{-R_f}{R}\right)}$$

Analog to Digital Circuit :-

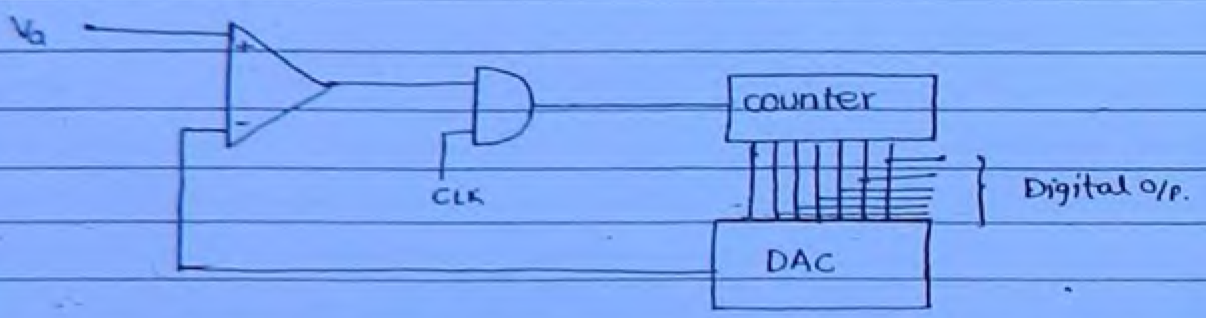
(A) Counter type ADC :-



$V_1 > V_2 \Rightarrow V_0 = V_{ref}$

$V_1 < V_2 \Rightarrow V_0 = -V_{ref}$

⇒ It is one bit quantizer.



⇒ In counter type ADC a comparator is used in I/p stage to compare I/p analog voltage with reference volta provided by DAC feedback.

⇒ A counter is used to count no. of clock pulses appli

⇒ when analog voltage (Va) is greater than DAC voltage then o/p is 1 then counter count and if analog voltage (Va) is less than reference voltage (DAC voltage) then o/p is 0 and counter stops counting and it give the comparative digital o/p.

⇒ Max. no. of clock pulses required for N bit conversion is $2^n - 1$.

⇒ Max. conversion time $= (2^n - 1)\, T_{CLK}$.

⇒ Conversion time depends on I/p analog voltage.

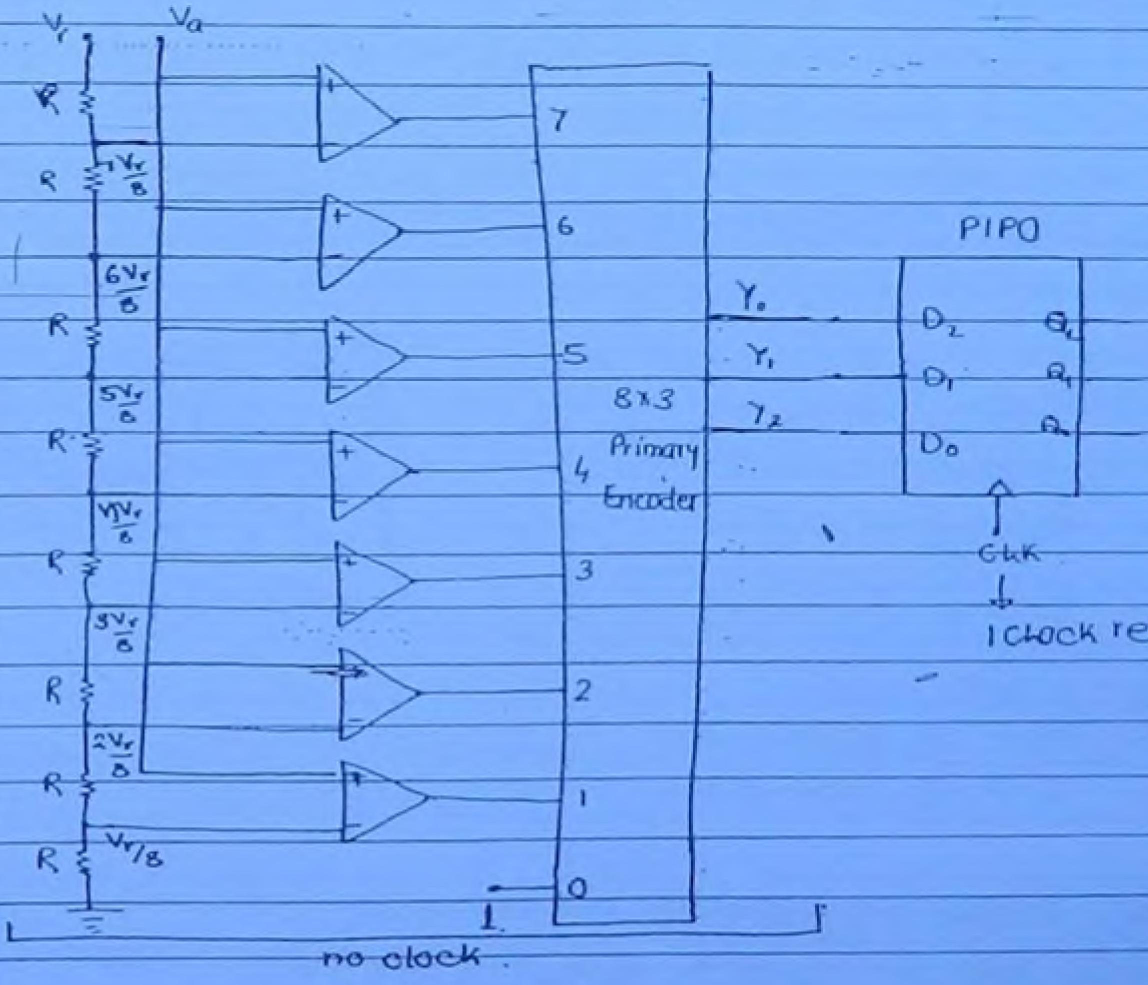
⇒ Also called Ramp type ADC

(B) Parallel comparator type :-

⇒ For n bit → 2^n-1 comparator required.
→ 2^n resistor required.
→ $2^n \times n$ priority encoder.

⇒ Also called Flash ADC (fastest ADC).

(B.1) 3 Bit parallel comparator :-



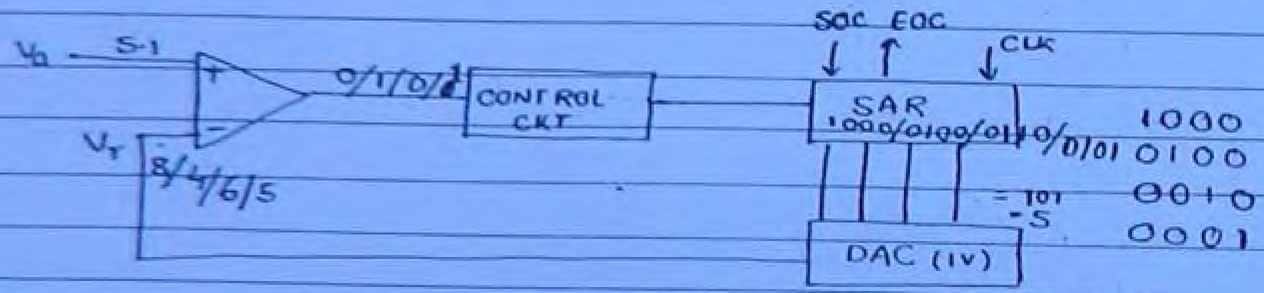
⇒ No clock pulse is required.

⇒ Therefore it is fastest. ADC among all.

⇒ Max no. of clock pulse required for n bit conversion is which is Inside PIPO.

Range of analog	O/P.
$V_a > 7V_r/8$	111
$7V_r/8 > V_a > 6V_r/8$	110
$6V_r/8 > V_a > 5V_r/8$	101
$5V_r/8 > V_a > 4V_r/8$	100
$4V_r/8 > V_a > 3V_r/8$	011
$3V_r/8 > V_a > 2V_r/8$	010
$2V_r/8 > V_a > V_r/8$	001
$V_r/8 > V_a$	000

(c) SAR Type (Successive ~~ty~~ approximation Register) :-



SOC - Start of conversion
EOC - End of conversion

⇒ Ring counter is used to set the base
⇒ Control ckt is used to reset ($V_a < V_r$)

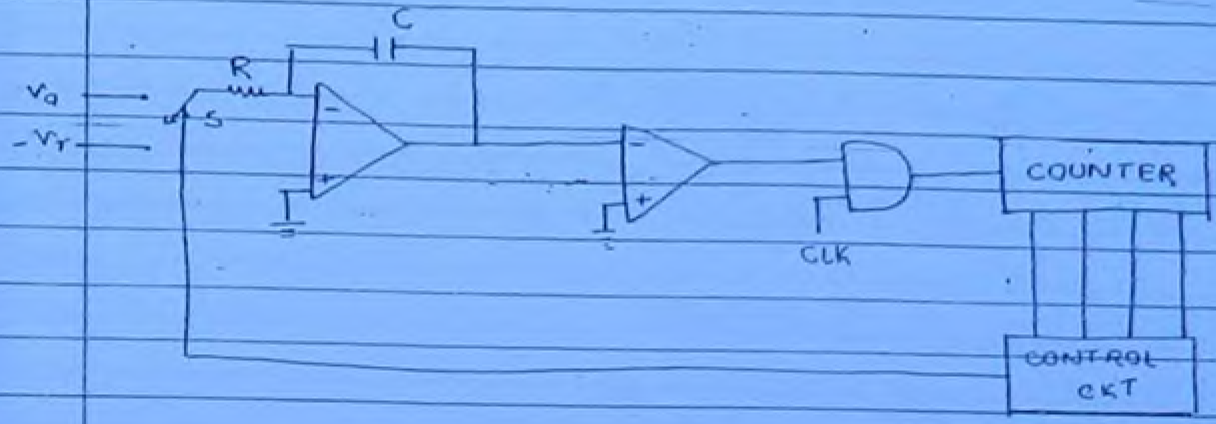
⇒ In SAR Type ADC, ring counter will present to successively set the base.
⇒ Control ckt is used to reset previously set bit when $V_a < V_r$.
⇒ In SAR Type ADC, n clock pulse required for n bit conversion.
⇒ $\boxed{\text{conversion time} = nT_{CLK}}$

⇒ SAR Type, conversion time uniform for any analog voltage (conversion time is independent of

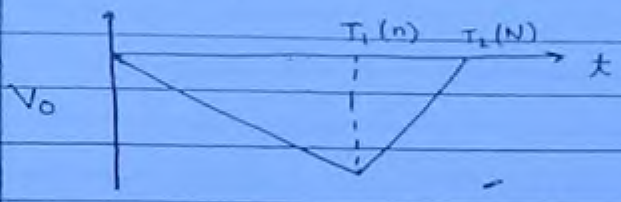
⇒ SAR is mostly used in Digital ckt to provide interface with microprocessor.

(152)

(D) Dual slope Integrating type ADC :-



⇒ V_r slope is always greater than V_a slope.



$T_1 = 2^n T_{CLK}$
$T_2 = N T_{CLK}$

⇒ In Dual slope a counter is used to count clock pulse

⇒ convesion started initially counter is reset to zero and switch s is connected to V_a (analog voltage) wh integrater is integrating analog voltage o/p of integrate will becom -ive voltage. due to this comparator o/p i 1. and counter continues clock pulses. after 2^m clk pulses again counter value become zero. at this time t_1 control ckt conect switch S to $-V_e$. During V_R integration upto T_2 time o/p of integrator is -ive. due to this counter again contin clock pulses. at time T_2 o/p of integrator become +i and comparator o/p become 0 due to this counte

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will stops. Let N is count when counter stops:

Then,

$$V_o = -\frac{V_a}{RC} . T_1 + \frac{V_r}{RC} (T_2 - T_1)$$

at time $t = T_2$, $V_o' = 0$.

$$\Rightarrow 0 = -\frac{V_a}{RC} . T_1 + \frac{V_r}{RC} (T_2 - T_1)$$

$$\Rightarrow V_a T_1 = V_r (T_2 - T_1)$$

$$\Rightarrow V_a \cdot 2^n \cdot T_{CLK} = V_r (N T_{CLK})$$

$$\Rightarrow N = \frac{V_a \cdot 2^n}{V_r} = \frac{V_a 2^n}{V_r}$$

$$\Rightarrow V_a = \frac{V_r}{2^n} . N.$$

$$\boxed{V_a = \frac{V_r}{2^n} . N}$$

if $V_r = 2^n$ then.

$$\boxed{V_a = N}$$

⇒ This is the most accurate ADC among all.

⇒ All ripple and noise is seperated or compressed by capacitor. (Therefore this have more accuracy due to integrator).

⇒ max. no. of clock pulse $=$ ~~2^n~~ $2^n - 1$.

$\approx 2^n + 2^n = 2^{n+1}$.

⇒ It is slowest among all.

Application :-

⇒ Mostly used in digital voltmeter.

Clock pulse :-

(i) counter type $= 2^n - 1$ (iii) Flash = 1

(ii) SAR $= n$ (iv) Dual type $= 2^{n+1}$

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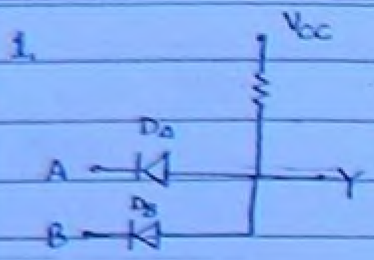
PAGE

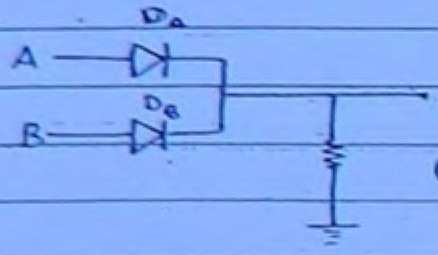
1.



(Diode AND Gate).

A	B	D_A	D_B	Y
0	0	ON	ON	0
0	1	ON	OFF	0
1	0	OFF	ON	0
1	1	OFF	OFF	1.

2.

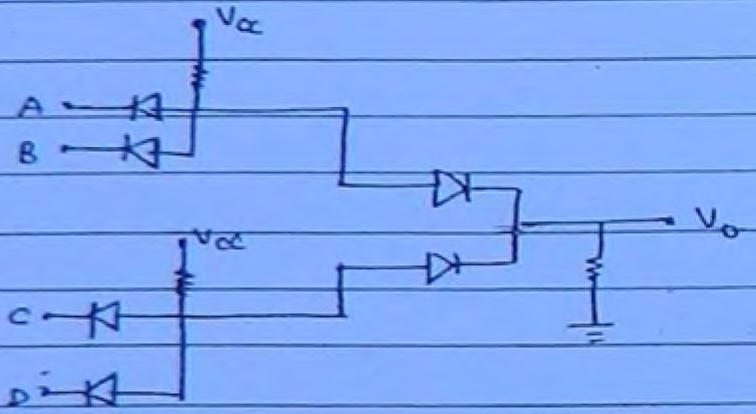


$V_o = A+B$

(Diod OR Gate)

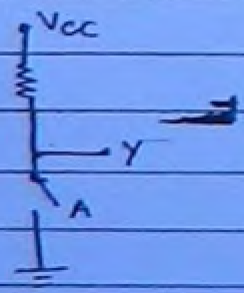
⇒ For Not gate we use transistor.

lem:-

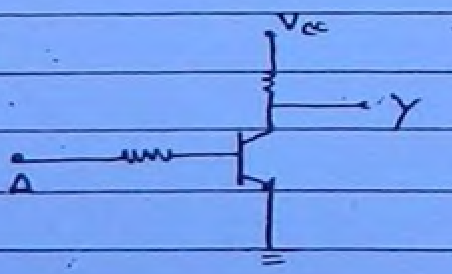


:- $V_o = AB+CD$.

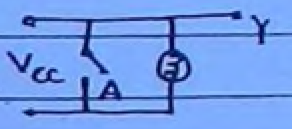
3. NOT :-



⇒



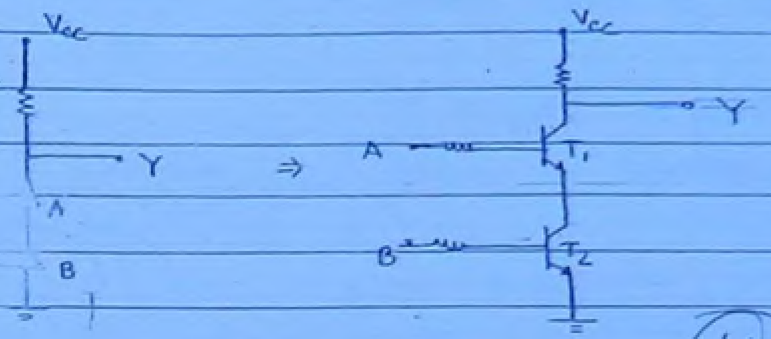
⇒



if A = 0, Tr is cutoff, Y = 1.

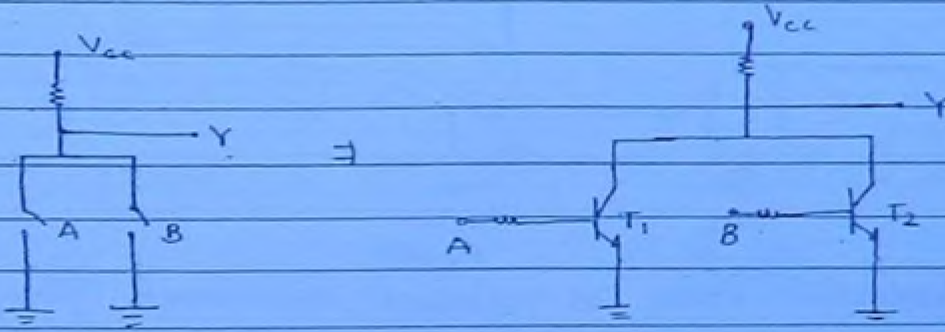
if A = 1, Tr is SAT, Y = 0

4. NAND Gate :-



A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

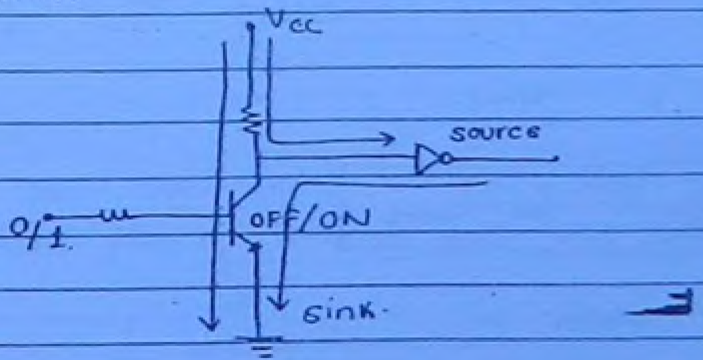
5. NOR Gate :-



A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

⇒ when logic gate o/p is 1. (Tr. OFF) it will act as current source.

⇒ when logic gate o/p is 0 (Tr. ON) it will act as current sink.



⇒ In cutoff and saturation region transistor will act as switch.

J_E	J_C	Region
RB	RB	cutoff
RB	FB	Reverse active
FB	RB	Active
FB	FB	SATURATION

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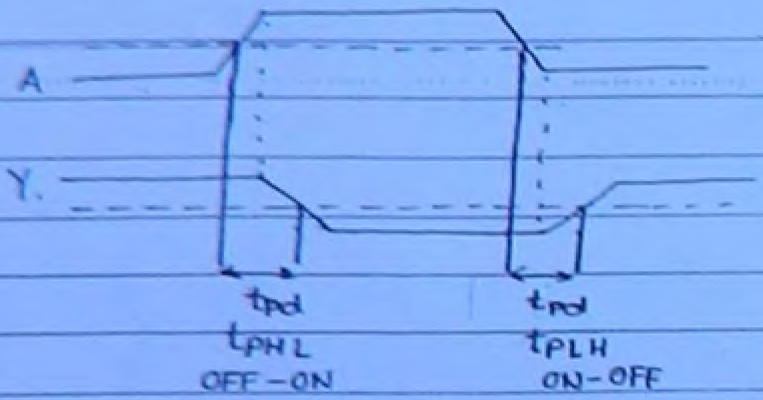
Characteristics of logic family :-

(i) Propagation delay :- (t_{Pd}) :-

⇒ It is measured in nsec.



$$\boxed{t_{Pd} = \frac{t_{PHL} + t_{PLH}}{2}}$$

⇒ Propagation delay is always measured from 50% value of the diag.

⇒ In Tr, ON to OFF time is more compare to OFF to ON time due to saturation or storatge time.

(ii) Power dissipation :-

⇒ Power dissipation by each logic gate.

⇒ P_{diss} = mW.

$$\boxed{P_{diss} = V_{cc} \cdot I_{cavg}}$$

(iii) Figure of Merit :-

$$\boxed{FOM = P_{diss} * t_{Pd1}} = \text{PJoule.}$$

⇒ I^2L have best FOM.

⇒ value of FOM is low the logic family is best

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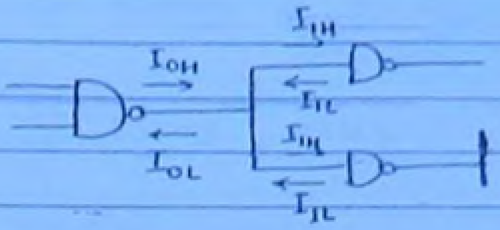
(iv) Fan out :-

It is max. no. of logic gate that can be given by to logic gate.



$$fanout_H = \frac{I_{OH}}{I_{6IH}}$$

$$fanout_L = \frac{I_{OL}}{I_{IL}}.$$

⇒ Max. fan out is min value of ($fanout_H$, $fanout_L$).

Ques:- if $I_{OH} = 400 \mu A$, $I_{IH} = 40 \mu A$, $I_{OL} = -16 mA$, $I_{IL} = 1.6$ find fanout.

Sol'. $$fanout_H = \frac{400}{40} = 10$$

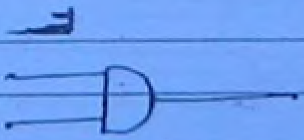
$$fanout_L = \frac{16}{1.6} = 10.$$

$$max.\ fan\ out = (10, 10)_{min} = 10.$$

⇒ TTL have max. fanout.

(v) Noise Margin :-

It is the max. noise voltage that can be added to the logic family which will not affect the o/p.



V_{IL} ← 0   0 → V_{OL}

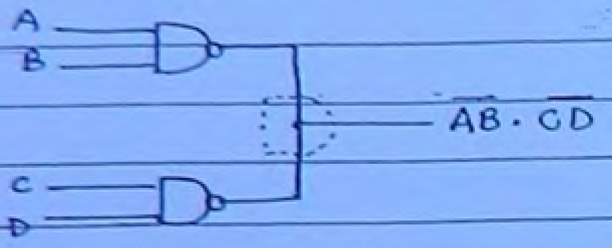
V_{OIH} ← 1   1 → V_{OH}

$$\boxed{\underbrace{V_{OH} > V_{IH}}_{\text{highleve. } NM_H} > \underbrace{V_{IL} > V_{OL}}_{\text{Low level } NM_L}}$$

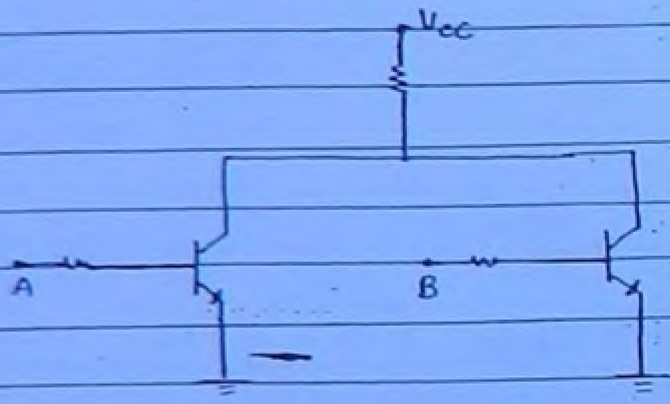
NM_H	=	$V_{OH} - V_{IH}$
NM_L	=	$V_{IL} - V_{OL}$

overall noise margin = $(NM_H, NM_L)_{min}$.

(A) RTL (Register Transistor logic) family :-



(wired AND)



- ⇒ Basic gate - NOR gate.
- ⇒ t_{pd} = 50ns.
- ⇒ P_{diss} = 10 mw.
- ⇒ FOM = 500 PJ
- ⇒ NM = 0.2 V
- ⇒ Fanout = 3
- ⇒ wired AND used.

Disadvantage :-

1. lower speed of operation.
2. low Noise margin
3. lowest fan out.

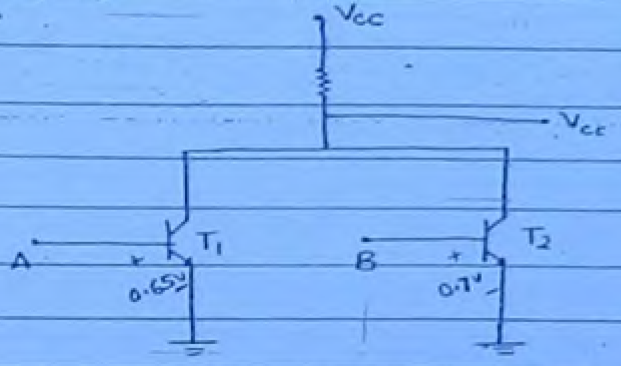
(B) DCTL (Direct Coupled Transistor logic) :-

⇒ In RTL logic family if I/P resistance removed then resultar is DCTL.

⇒ t_{pd} = 40nsec.

Disadvantage :-

⇒ Current Hogging.



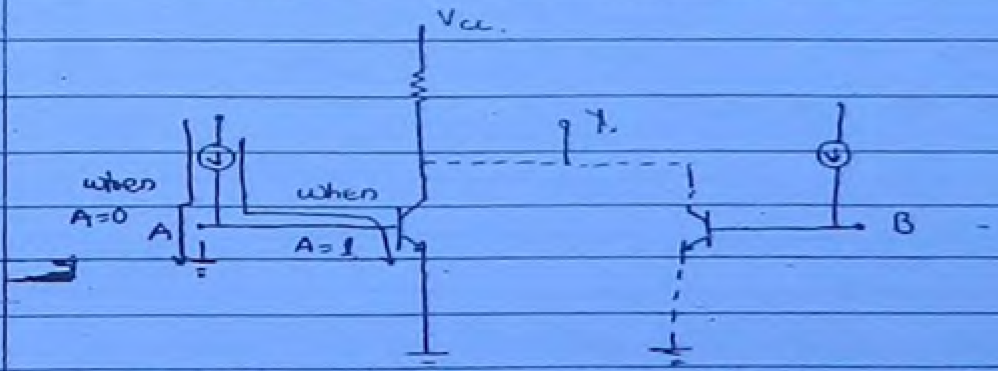
A	B	T₁	T₂	Y
0	0	OFF	OFF	1
0	1	OFF	ON	0
1	0	ON	OFF	0
1	1	ON	OFF	0

due to current Hogging

⇒ In DCTL logic, If tr. switch different characteristics are use the Tr having lower V_{BESAT} then first ON and it will no allow other Tr to ON. this phenomenon is known as curre Hogging.

Integrated Injection logic (I^2L) :-

⇒ It's injecting the current into Base.



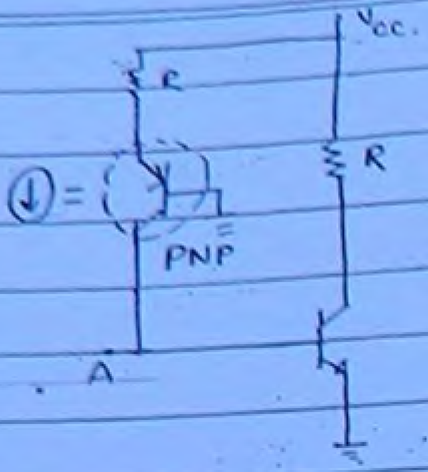
⇒ When A is high the current flows through the base of Tr.

⇒ i.e. T₁. must be ON.

⇒ I^2L covers less space.

⇒ ie I^2L have high density.

⇒ It is equivalent to NOT gate.



⇒ There is no problem of current Hogging.

⇒ FOM = 0.1 PJ – 0.7 PJ.

Best FOM among all logic family.

⇒ t_{pd} = 40ns.

⇒ Fan out = 8.

SSI – 1-12
MSI – 13-99
LSI – 100-1000
VLSI – > 1000.

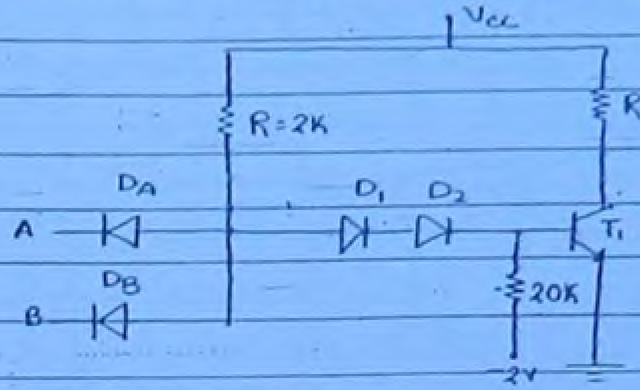
} no of gates used in this integration.

⇒ In I^2L logic, due to integration of PNP and NPN tr. it occupies less area hence density are more in I^2EL logic. It is mostly used in MSI and LSI logic family.

⇒ Also called MTL (Merged logic family) due to integration of Transistor.

DTL (Diode Transistor logic) family :-

⇒ AND Gate followed by NOT gate.



A	B	T_1	Y
0	0	OFF	1
0	1	OFF	1
1	0	OFF	1
1	1	ON	0

⇒ 20K resister used only for discharging the junction capacitance. The capacitance which is discharge is Transition cap. C_c.

⇒ The ckt is called Basic DTL gate.

⇒ In this any one of the I/P is low. or all the I/P are low, D_A ~~and~~ or D_B will become forward bias where as D_1 and D_2 will become reverse bias. due to tt Tr T_1 is OFF and O/P is 1.

⇒ when all the I/P's are high then D_A and D_B become reverse bias and D_1 and D_2 will become forward bias and T_1 is ON and O/P is low.

⇒ The basic gate is NAND gate.

⇒ t_{Pd} = 30ns.

⇒ P_{diss} = 8mw.

⇒ FOM = 240 PJ

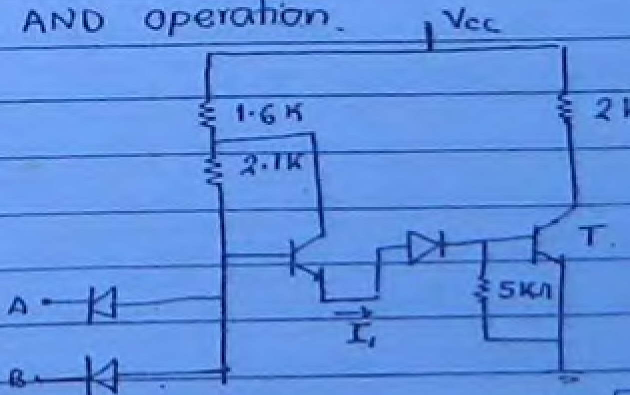
⇒ NM = 0.75 V

⇒ Fanout = 3.

⇒ It provides wired AND operation.

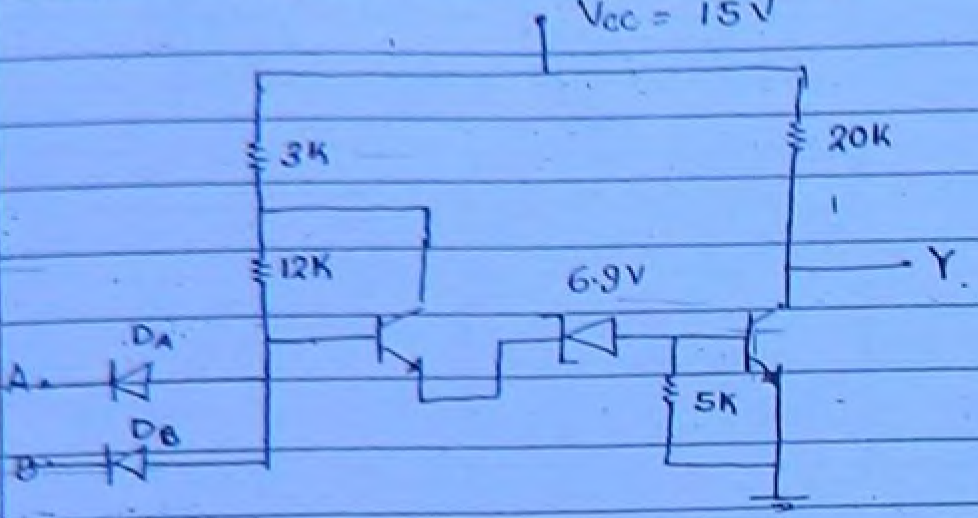
⇒ To increase fan out we introduce Tr in place of Diode.

⇒ 5KΩ resistor used to lower the I_1 current.



called STANDARD LOGIC

High Threshold logic (HTL) family :-



⇒ Zener Diode is used in place of D_2

⇒ NM = 4 - 5V (Highest noise margin)

⇒ since in DTL all diode and Transistor is -ive temp coefficient (· $\frac{dv}{dT}$ = $\ominus$ - 2.5 mv/°C.

⇒ logic 0 = 2V
logic 1 = 12V.
} Higher voltage swing

⇒ t_{pd} = 90 ns

⇒ P_{diss} = 55 mw

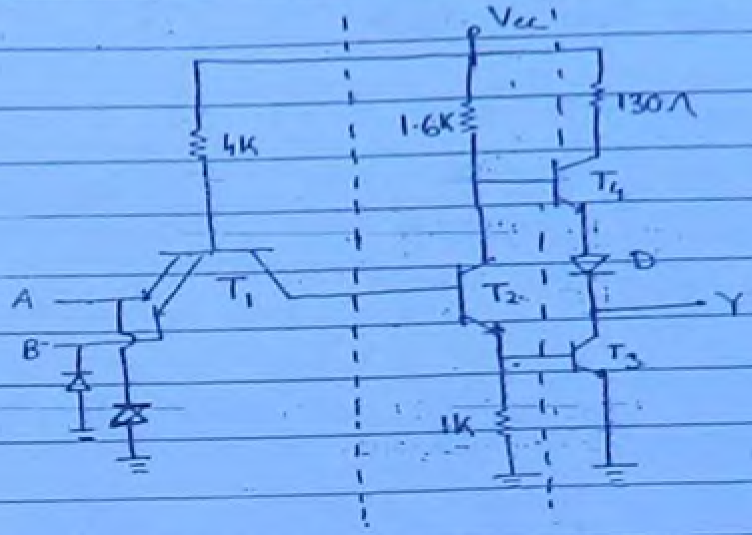
⇒ FOM = 4950 PJ ≈ 5000 PJ.

⇒ Fanout = 8

⇒ Basic gate = NAND gate.

⇒ Noise margin = 4V - 5V.

TTL (Transistor Transistor logic) family :-



T_1 = Multiemitter transistor.

A	B	T_1	T_2	T_3	T_4	Y
0	0	A	C	C	S	1
0	1	A	C	C	S	1
1	0	A	C	C	S	1
1	1	R	S	S	C	0

⇒ The ckt shown in fig. is standard TTL logic family. it basically have three stage.

(i) Multiemitter I/P stage

(ii) Phase splitter.

(iii) Totem pole or, active pull up. O/P stage.

active = use of Tr T_4

Pullup = Tr (T_4) connect to Vcc.

Operation :-

⇒ Any one of I/P low or all I/P's are low then EB junction is FB. (J_E = FB) and collector base (J_C = RB junction is RB . Tr. is in active mode. due to this Tr. T_2 and T_3 are OFF (in cutoff region) where as T_4 in is SAT . Hence O/P is 1.

⇒ When all the I/P's are high then J_E (EB Junct^n) of T_1 is RB. and J_C (CB Junct^n) is FB. (The mode of operation is Reverse active. —

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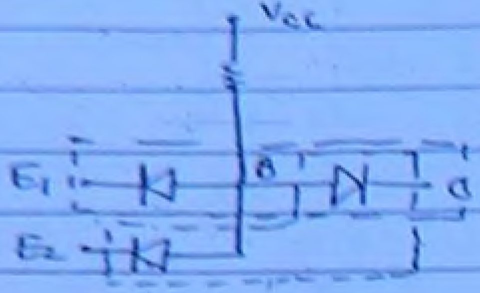
T_2 and T_3 are in saturation and T_4 is in cutoff. Hence o/p is zero.



(170)

V_{IH} = 2 V → I/p voltage at which Tr. takes logic

V_{OH} = 2.4 V

V_{IL} = 0.8

V_{IH} = 0.4

t_{pd} = 10 ns

P_{diss} = 10 mw

FOM = 100 PJ

Fanout = 10

NM = 0.4V

⇒ Diode D is used to cutoff Tr T_4 when T_3 is ON.

⇒ Advantage of Totem pole :-

1. lower power dissipation.
2. Higher speed of operation.
3. Higher fan out.

⇒ Disadvantage of Totem pole :-

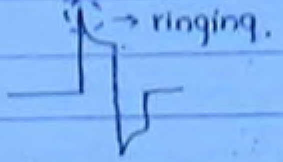
It is not used in wired logic

⇒ To provide wired AND logic open collector configuration is used.

⇒ 130 Ω resistor used in collector in O/P statge to reduce ripple or noise generation. to in fr high frequency of operation.

⇒ In TTL if any I/P is open it behaves as logic 1.

⇒ Clamping diodes are connected in I/P stage to prote transistor during high frequency of operation.



⇒ clamping D. removes ringing of high frequency operation.

⇒ There are different type of TTL:-

(a) standard TTL
(b) High speed
(c) low power
(d) Schottky TTL.

High speed TTL :-

In standard TTL logic family if Resistor value reduce then t_{pd} reduces and known as High speed logic family.

$t_{pd} = 6nsec.$

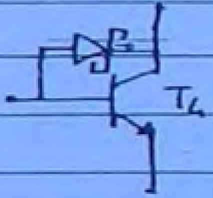
⇒ Power dissipation increases.

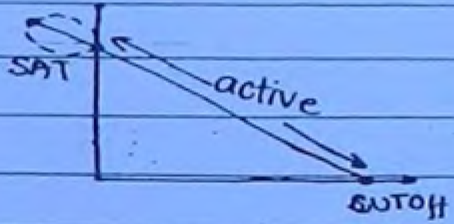
low speed power TTL :-

In TTL logic family if Resistor value increased then power dissipation reduced and resultant is known as low power logic family.

Schottky diode :-

If schottky diode is used b/w collector and Base region then it will remove storage time and saturation delay. the family known as schottky diode TTL.





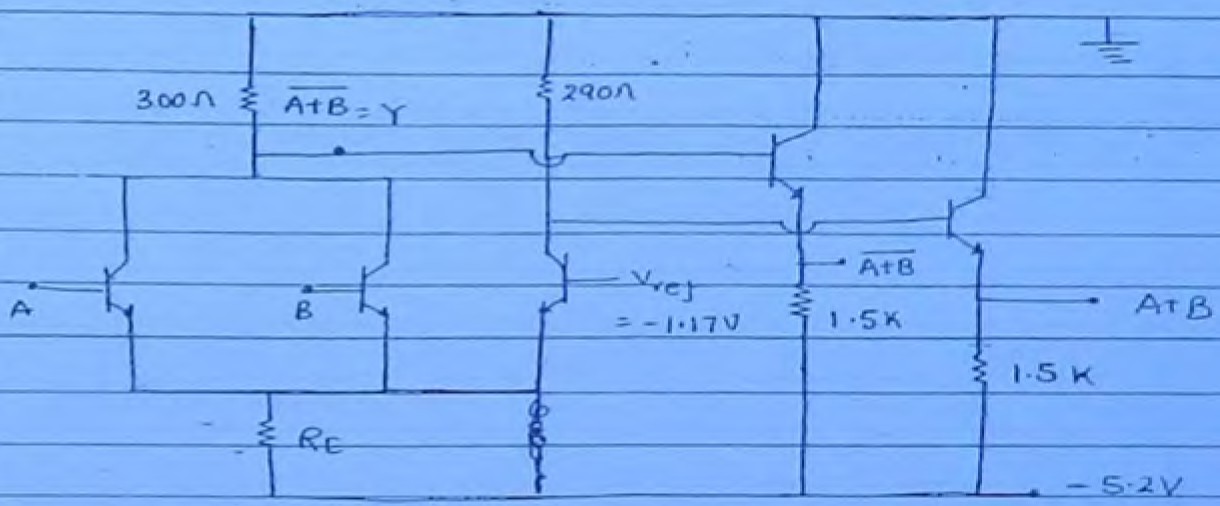
$t_{pd} = 2nSec.$

ECL (Emitter coupled logic family) :-

⇒ It is never go in saturation region.

⇒ work only in cutoff and Active region.

⇒ It is fastest logic family due to work in Active and cutoff region. (Because it is non saturated)



t_{pd} = 1nSec

fanout = 25.

⇒ It basically ~~contains~~ contains two stage.

(1.) Differential amp' I/P stage.

(2).- CC or Emitter follower O/P stage.

⇒ Due to use of D.A. complementry O/P are available in ECL logic family. (NOR / OR) gate.

⇒ Due to use of CC stage in the O/P fanout is high

⇒ Negative spikes do not affect the transistor due to -ive power supply.

⇒ ECL uses -ive power supply. Due to this any spikes or negative voltage not affect operation.

t_{pd} = 1nS

P_{diss} = 55mw

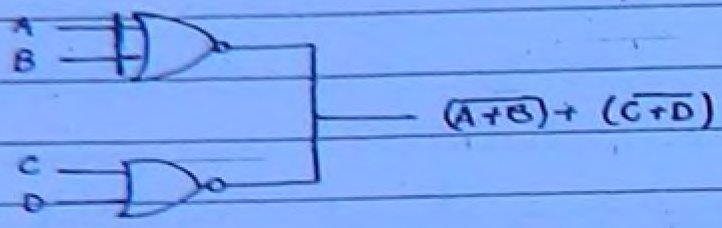
FOM = 55PJ

Fanout = 25

N.M = 0.3V

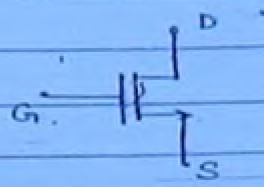
logic 0 = − 1.7V
logic 1 = − 0.85V } It is logic 1 made only voltage supply is negative.

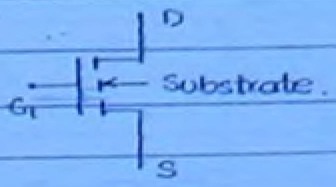
⇒ ECL provide wired AND logic



⇒ If any I/P is open then it is logic '0'.

NMOS :-

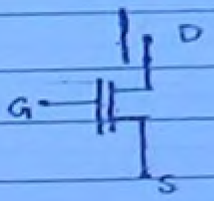




N-channel :-

logic '0' = OFF

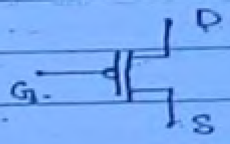
logic 1. = ON.



P- channel MOS :-

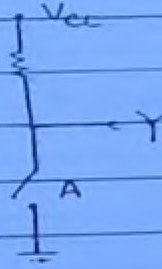
logic '0' = ON

logic 1 = OFF.

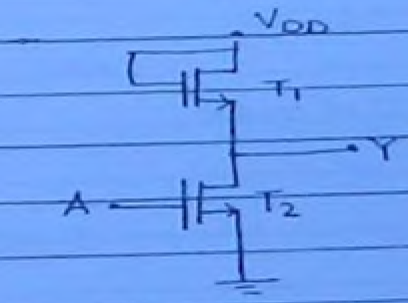


⇒ Since FET is voltage variable resistor hence in MOS circuit in place of ~~reg~~ resistor we use MOSFET.

NMOS NOT Gate :-

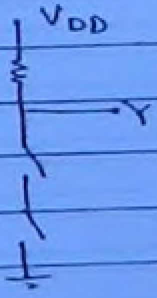


⇒

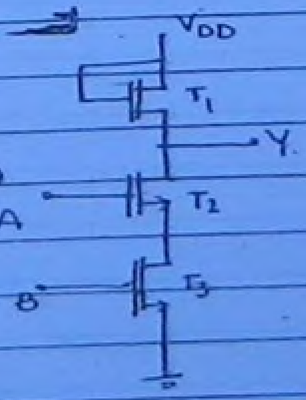


A	T_2	Y
0	OFF	1
1	ON	0

NMOS NAND Gate :-

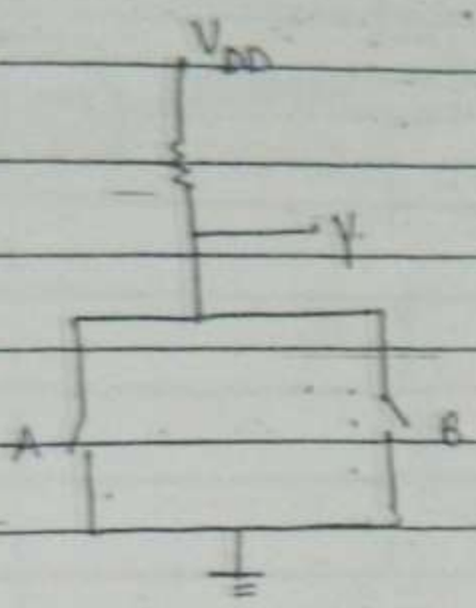


⇒

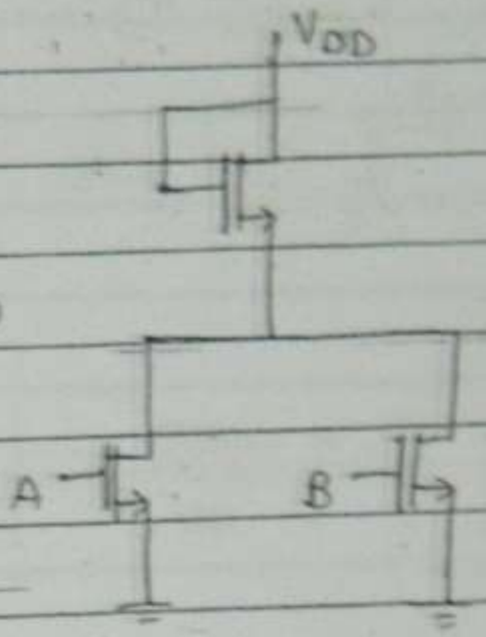


A	B	T_2	T_3	Y
0	0	OFF	OFF	1
0	1	OFF	ON	1
1	0	ON	OFF	1
1	1	ON	ON	0

NMOS NOR Gate :-



⇒



t_{pd} = 250 nsec

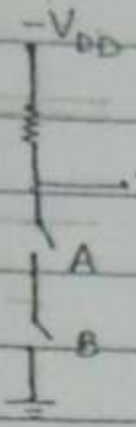
P_{diss} = 1mw

FOM = 250PJ

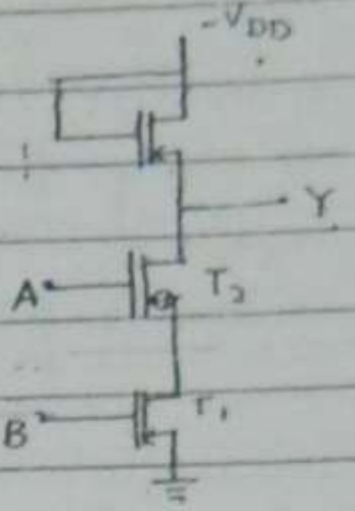
fanout = 5

NM = 1·5V

PMOS NOR Gate :-



⇒



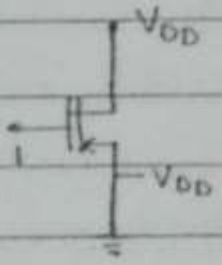
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

t_{pd} = 300 nsec

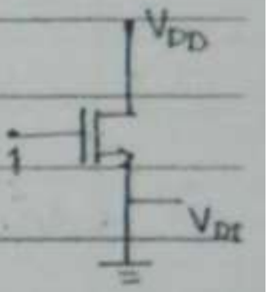
P_{diss} = 0.2 mW

FOM = 60 PJ.

PMOS → Strong in 1. → Weak in 0

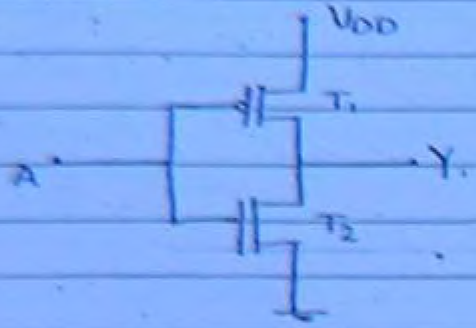


NMOS → Strong in 0 → Weak in 1.

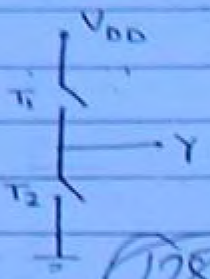


where, V_T = Threshold voltage.

CMOS NOT Gate :-

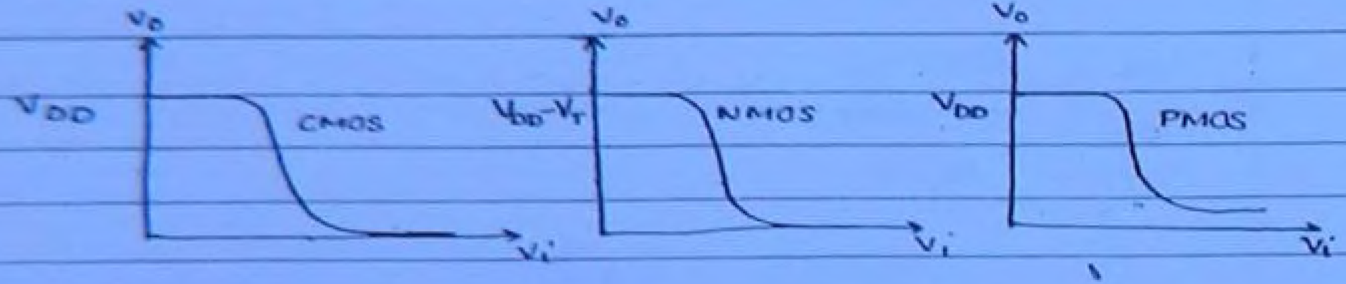


⇒



A	T_1	T_2	Y
0	ON	OFF	1
1	OFF	ON	0

Transfer characteristics :-



⇒ lowest power dissipation.

P_{diss} = 0.01 mw

t_{pd} = 70 nsec

FOM = 0.7 pJ

Fanout = 50

NM = $\frac{V_{DD}}{2}$

Power Dissipation :-

(i) Static PD =

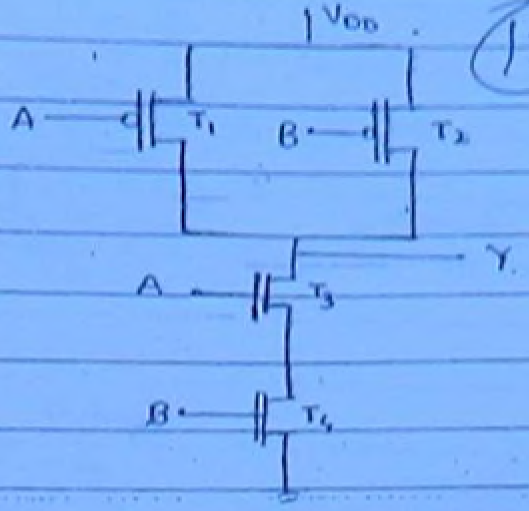
to During logic '0' or logic '1'.

(ii) Dynamic PD =

During transition from 0→1 or 1→0.

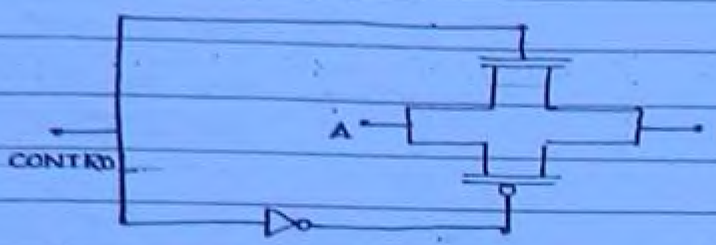
$$\boxed{PD = Cf V_{DD}^2}$$

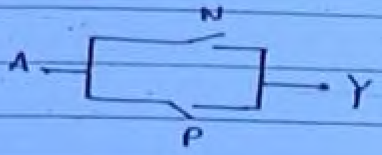
GMOS NAND Gate:-



A	B	T_1	T_2	T_3	T_4	Y
0	0	ON	ON	OFF	OFF	1
0	1	ON	OFF	OFF	ON	1
1	0	OFF	ON	ON	OFF	1
1	1	OFF	OFF	ON	ON	0

Transmission Gate :-

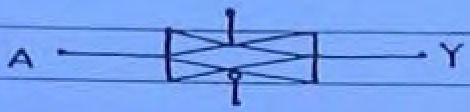


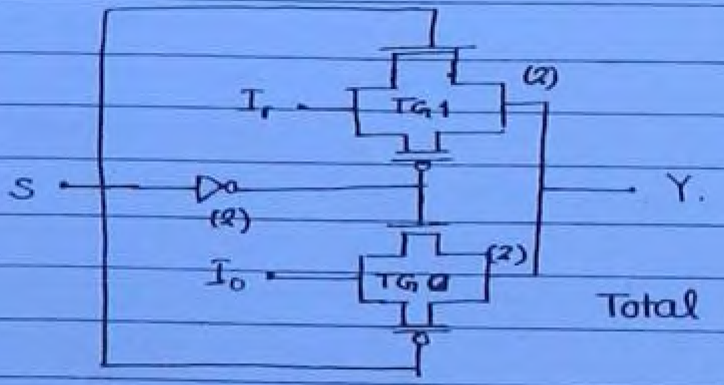


Control	A	Y
0	*	High impedence.
1	0	0
1	1	1

Control	Y
0	High imped
1	A

Symbol of Transmission gate :-

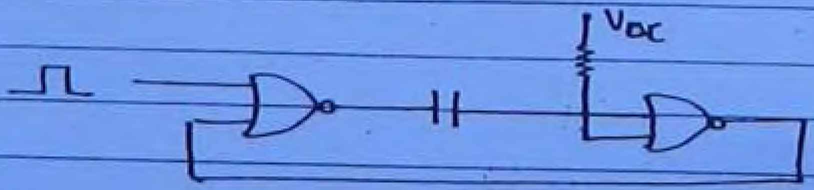




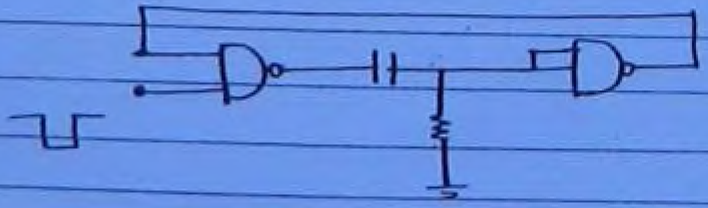
S	Y
0	I_0
1	I_1

Total no. of transistor
= 2+2+2 = 6.

CMOS monostable multivibrator :-



NAND



AND